Compal Confidential

M/B Schematics Document

Intel Skylake-H 4+2 + AMD Tropo XT2

LA-C951P

2015-08-14

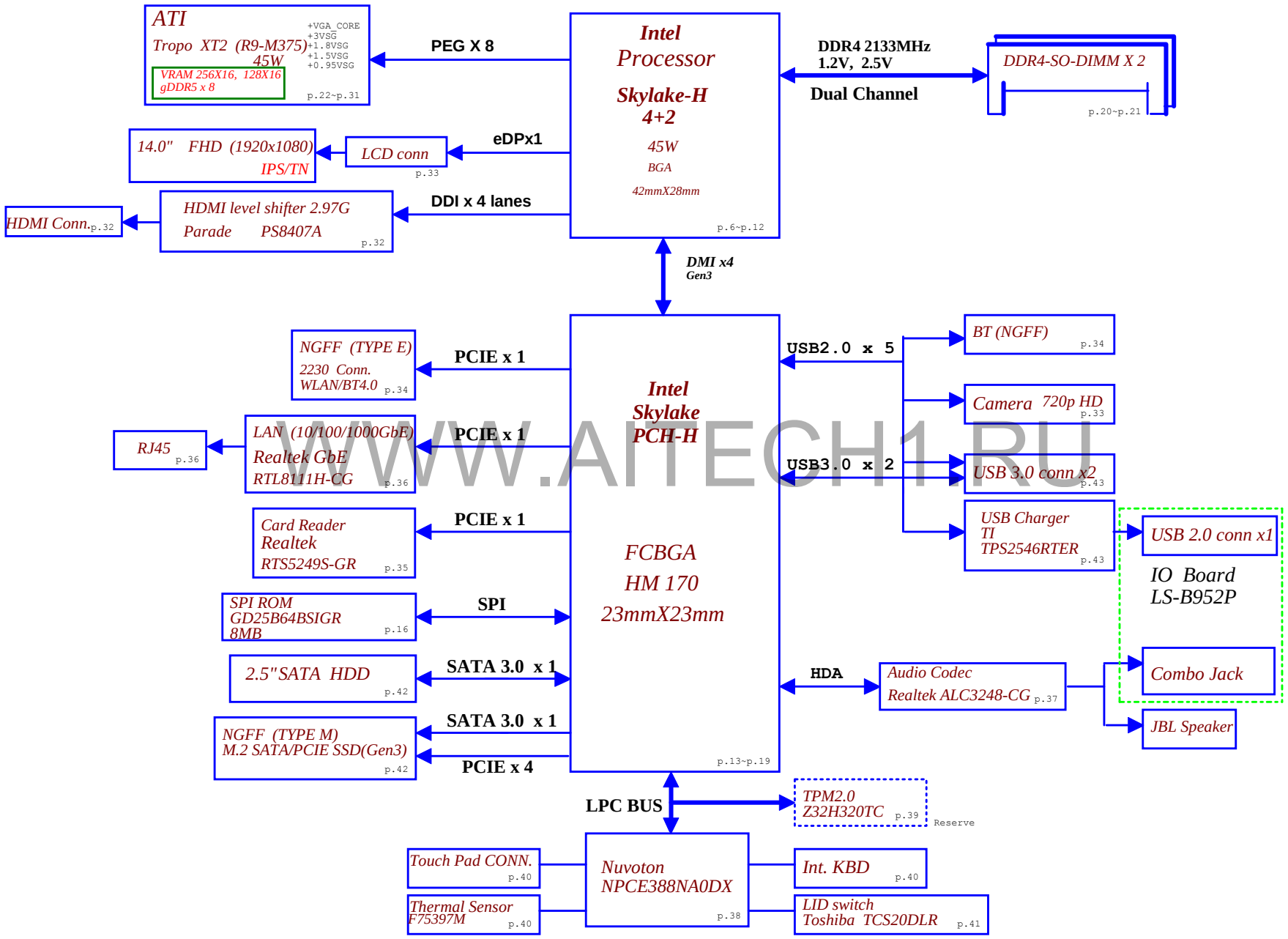
REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: LA-C951P	Rev: 1.0
Date: Friday, August 14, 2015	Sheet 1 of 62	

Compal Confidential
Model Name : AIPY6
Project Name : LA-C951P

Skylake-H



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Title: Block Diagram

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BOM Structure Table

Funct i on	Stuf f	Un-Stuf f
DGPU SKU	DIS@	@DIS@
SPI_IO3(MOW36)	QS@	ES@
2G VRAM	V2G@	
4G VRAM	V4G@	
NC Components		@
CMC		CMC@
TPM		TPM@
EMI	EMI@	@EMI@
ESD	ESD@	@ESD@
RF	RF@	@RF@
ISCT	NOISCT@	ISCT@
MPHY_EXT	NOEXTMPHY@	EXTMPHY@
CPU	CPU5@/CPU6@	
KB ID	NOKBL@/KBL@	

HSIO Port Table

HSIO Port	Capable	Device	PCIE CLK	NOTE
1	USB3.0_1 / OTG	NA		
2	USB3.0_2 / SSIC_1	NA		
3	USB3.0_3 / SSIC_2	USB3.0 (MB_UP)		
4	USB3.0_4	USB3.0 (MB_DOWN)		
5	USB3.0_5 / PCIE_1	NA		
....	....	....	....	
12	PCIE_6	WLAN(NGFF_KEY E)	CLK3	
....	....	....	....	
16	PCIE_10 / SATA_1A	HDD_SATA		
17	PCIE_11	Card Reader	CLK2	
18	PCIE_12	LAN	CLK1	
19	PCIE_13 / SATA_0B	SSD_SATA	CLK4	Opt i on SS D type
20	PCIE_14 / SATA_1B	SSD_PCIe x 4		
21	PCIE_15 / SATA_2			
22	PCIE_16 / SATA_3			
....	....	....	....	

USB2.0 Port Table

USB2.0 Port	Device
1	USB3.0 (MB_UP)
2	USB3.0 (MB_DOWN)
3	NA
4	BT (NGFF)
5	NA
6	USB2.0 (IO_Charge Port)
7	NA
8	Camera
9	NA
10	NA

ZZZ @
PCB 1F6 LA-C951P REV1 M/B 2
DA80013R010
ZZZ
PCB AIPY6 LA-C951P LS-C951P/C952P 02
DAZ1F600100

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA0
		DIMM2	TBC	TBC	0xA4
		TP	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS		TBC	TBC	TBC
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		Thermal sensor	1001100	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port 1	+3VLP	BAT	TBC	TBC	TBC
		CHGR	TBC	TBC	TBC
SMBUS Port 2	+3VLP	TP (reserve)	TBC	TBC	TBC
	+3VLP	Thermal sensor	1001100	TBC	TBC

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Descript i on	S0	S3	S4/S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Bat t ery po wer s uppl y	N/A	N/A	N/A
+19VB	AC or bat t ery po wer r ail f orpo wer circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Opt i on Tabl e

BOM Number	Load BOM Opt i on
4519YS38L09	DIS@/QS@/EMI@/ESD@/RF@/NOEXTMPHY@/HM170@/NOISCT@ /CPU5@/KBL@
4519YS38L12	DIS@/QS@/EMI@/ESD@/RF@/NOEXTMPHY@/HM170@/NOISCT@ /CPU6@/KBL@

CPU/PCH part

SKL-H
UC1 CPU5@
S IC CL8066202194632 SR2FP R0 2.3G C38!
SA000096Q30
UC1 CPU6@
S IC CL8066202194635 SR2FQ R0 2.6G C38!
SA000095Z50

PCH-H
UH1 HM170@
S IC GLHM170 SR2C4 D1 BGA 837P PCH C38 !
SA000096J60

VGA
UV1 DIS@
S IC 216-0866000 A1 TROPO XT2 962P C38!
SA00008B310

HDMI
HDMI
HDMI_ROYALTY
ROYALTY HDMI W/LOGO+HDCP 45@

gDDR5 VRAM * 8

2G X7663138L01

ZZZ V2G@
EDW2032BBBG-6A-F-R

Hynix_X76xxx38Lxx
H5TC2G63FFR-11C
SA00006H410

Micron_X7663138L01
EDW2032BBBG-6A-F-R
SA00007HS10

Samsung_X7663138L02
K4G20325FD-FC03
SA000066I10

4G X7663138L03

ZZZ V4G@
EDW4032BABG-50-F

Hynix_X7663138L04
H5GC4H24AJR-T2C
SA000085V40

Micron_X7663138L03
EDW4032BABG-50-F
SA00008VF10

Samsung_X76xxx38Lxx
K4W4G1646E-BC1A

10K_0402_5%

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Title: Notes List
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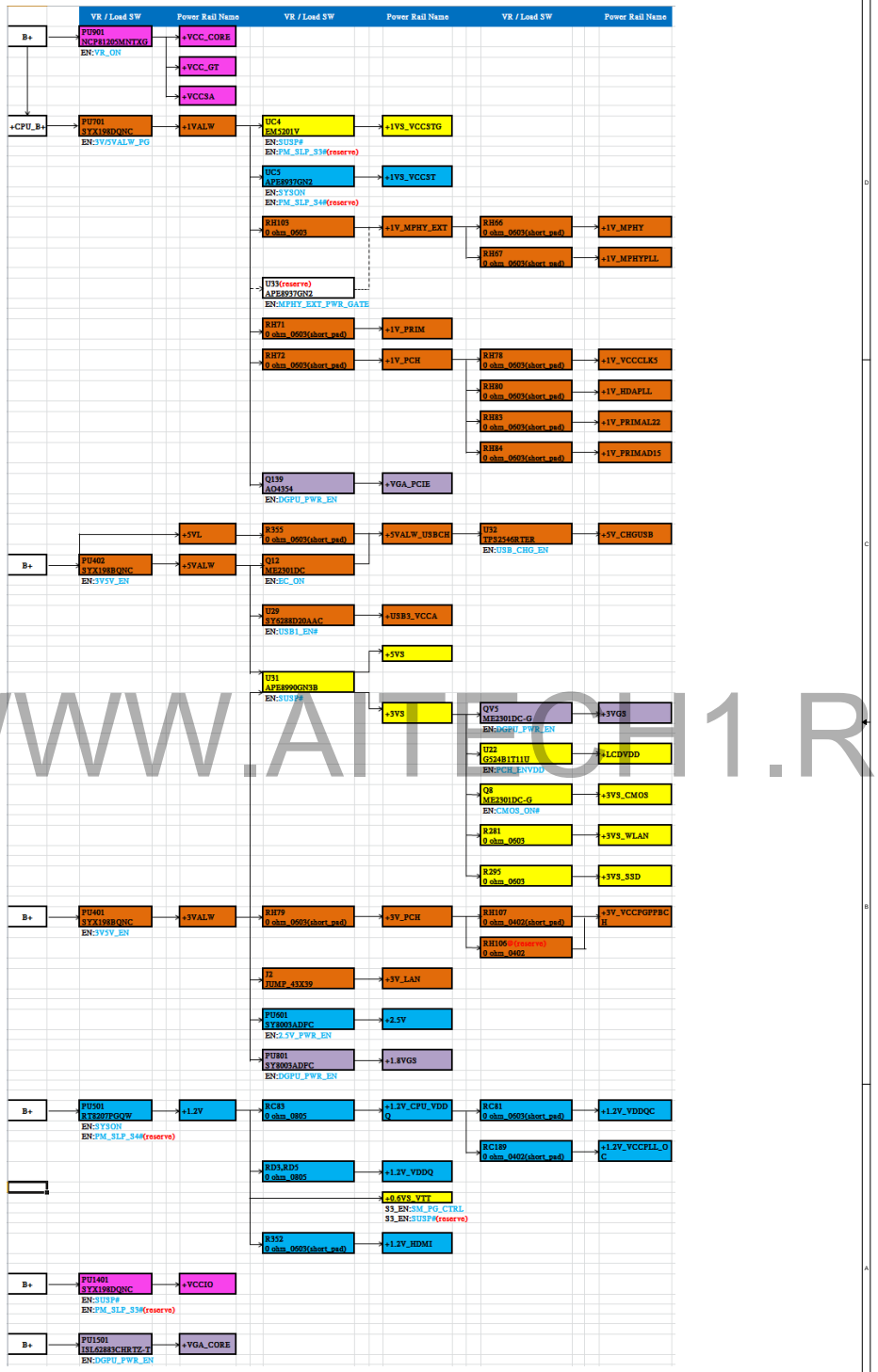

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Title: **Power map**

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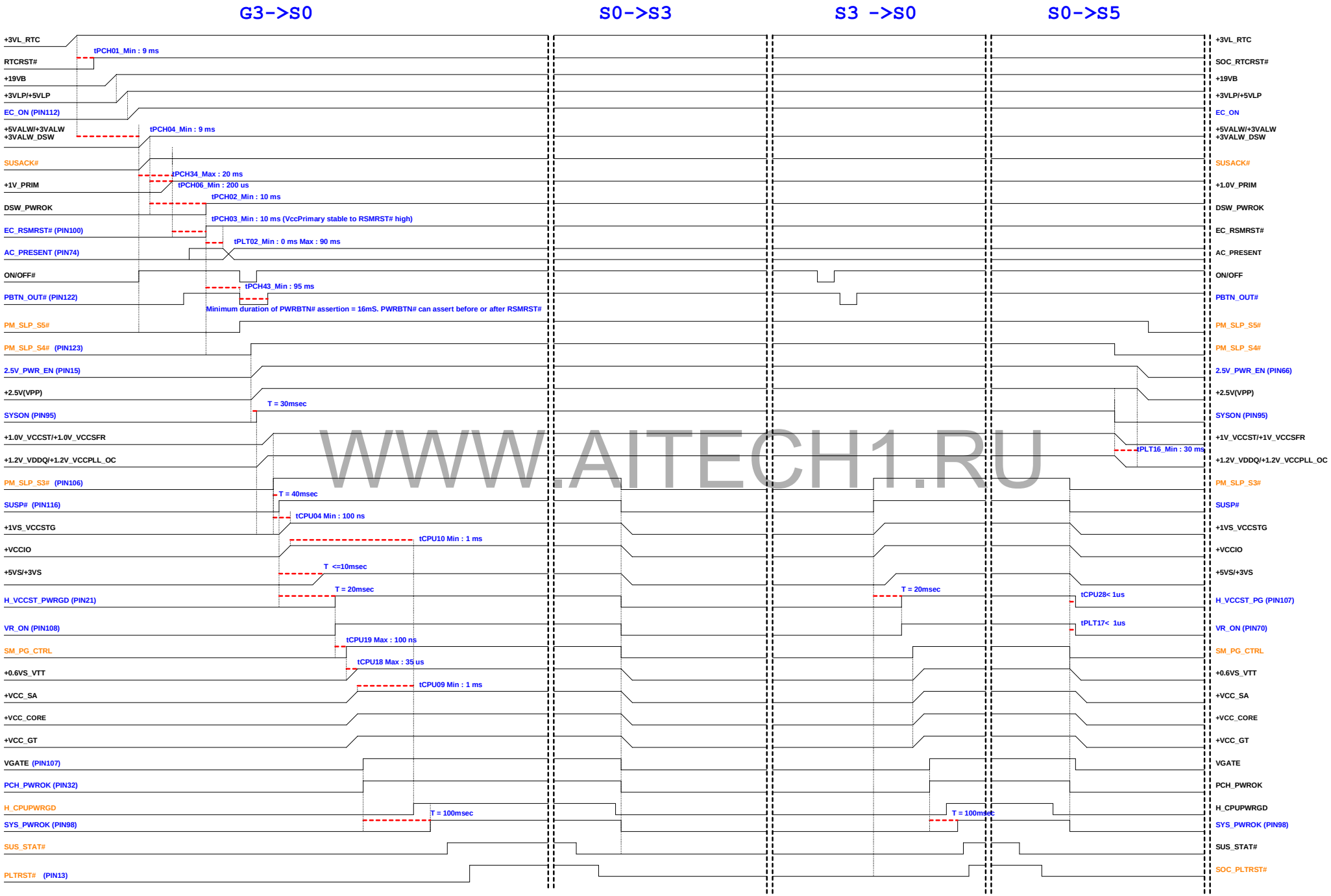
[AIPY6-PWR Sequence_SKL-H 4+2_DDR4]



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Compal Electronics, Inc.			
Title: Power Sequence			
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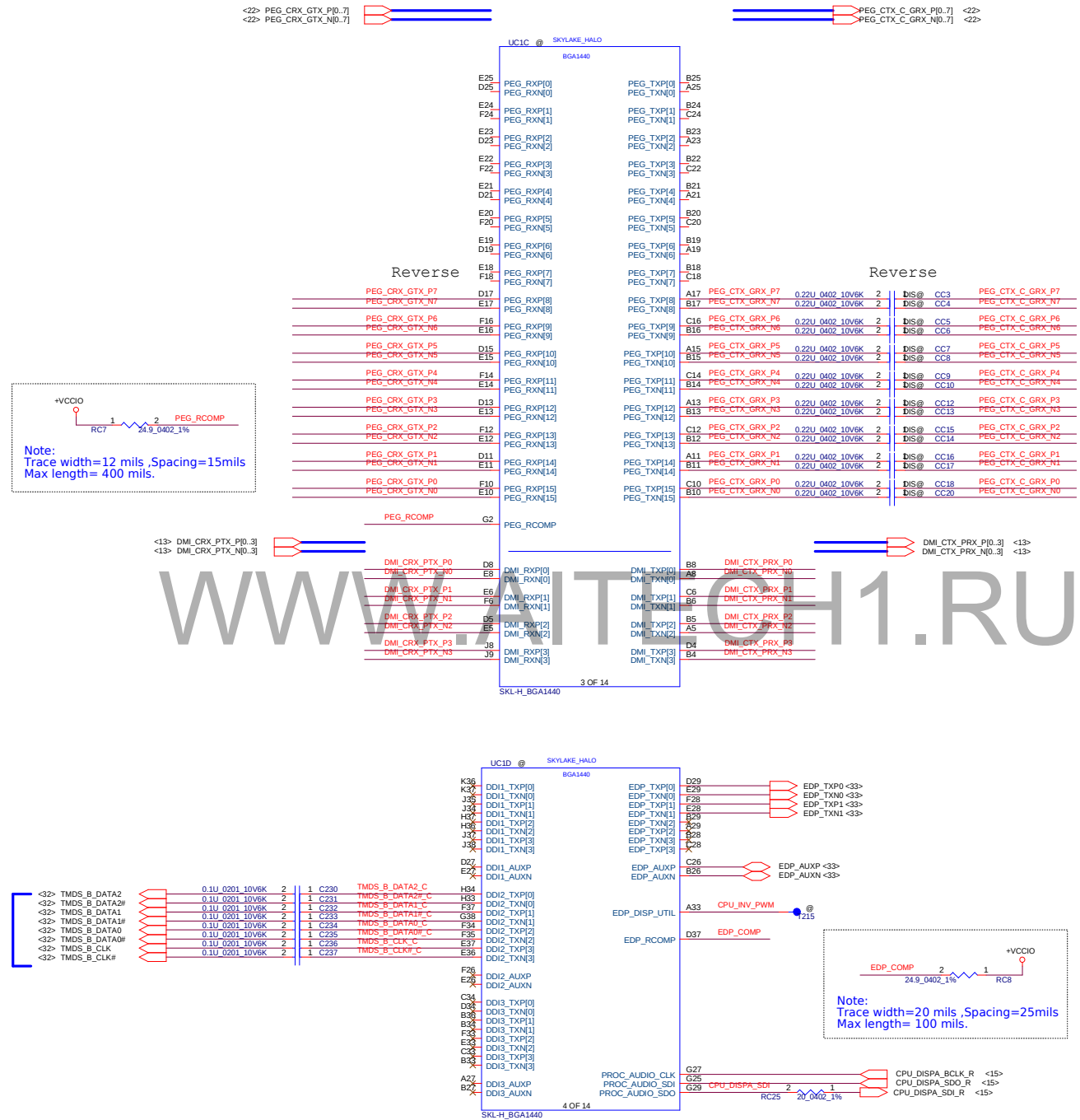

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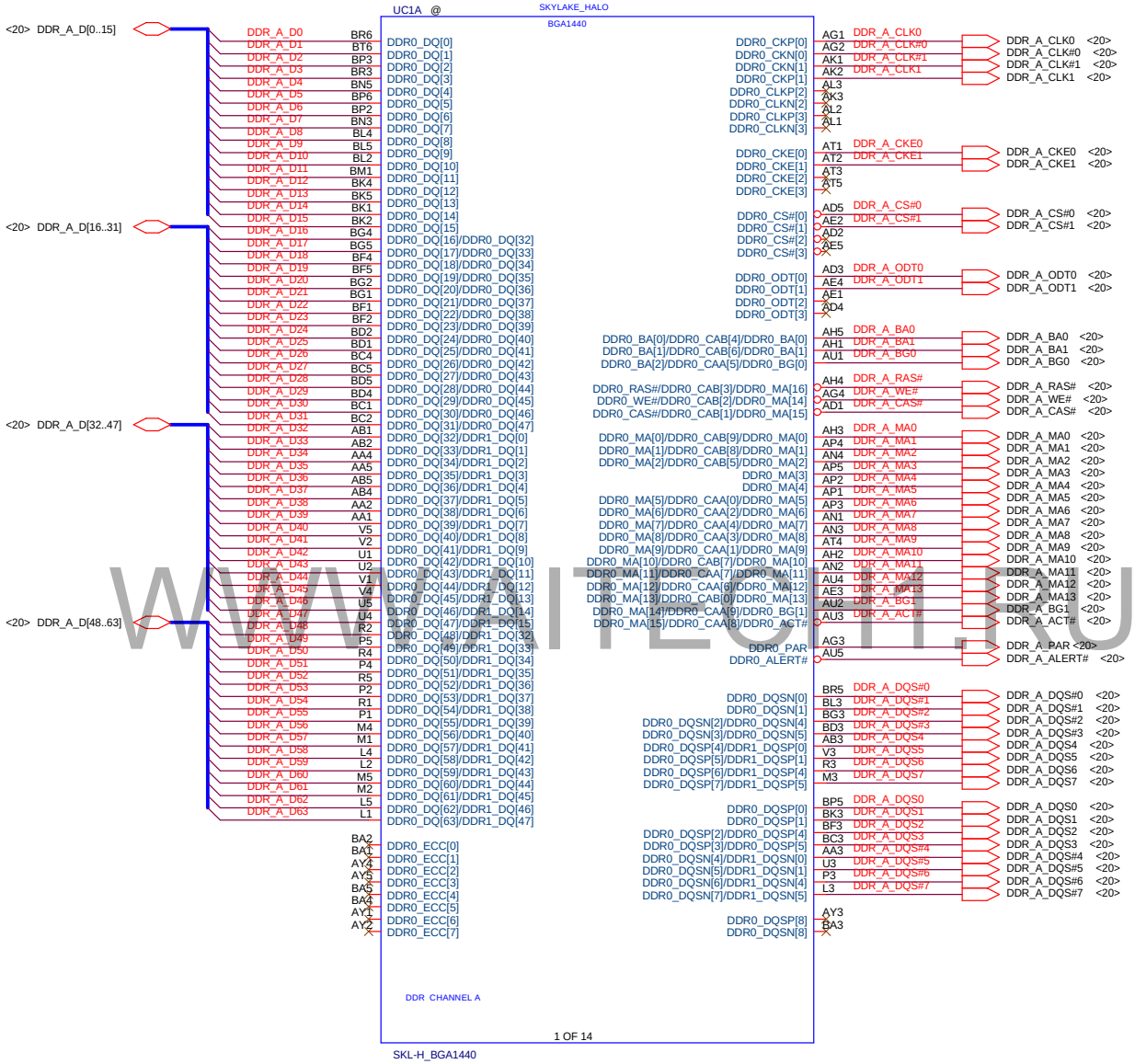
Title: DMI,PEG,DDI,EDP			
Size: Custom	Document Number: LA-C951P		Rev: 1.0
Date: Friday, August 14, 2015	Sheet 6 of 62		



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Title: **DDR4_CHA**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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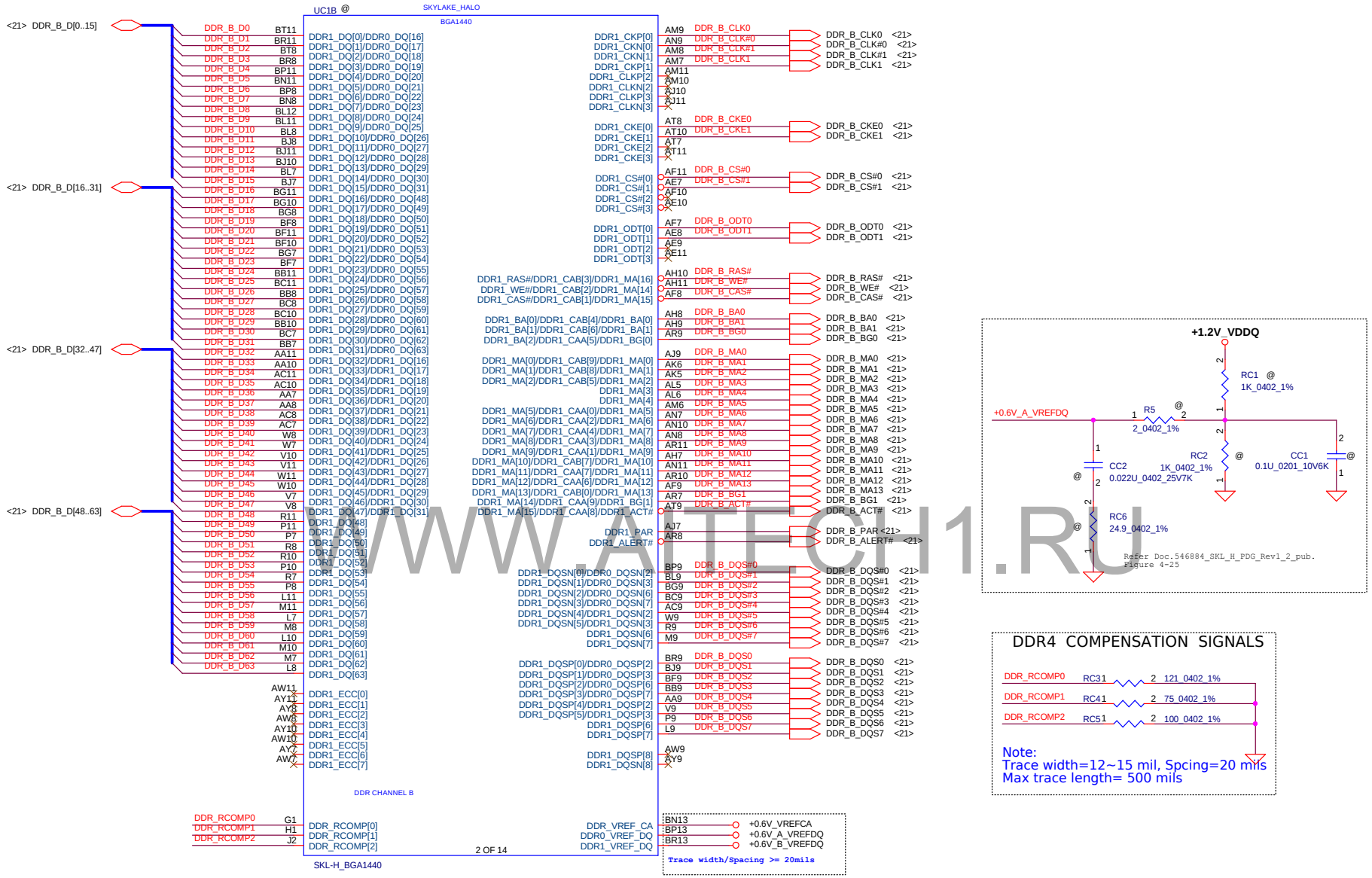

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Title: **DDR4_CHB**

Size	Document Number	Rev
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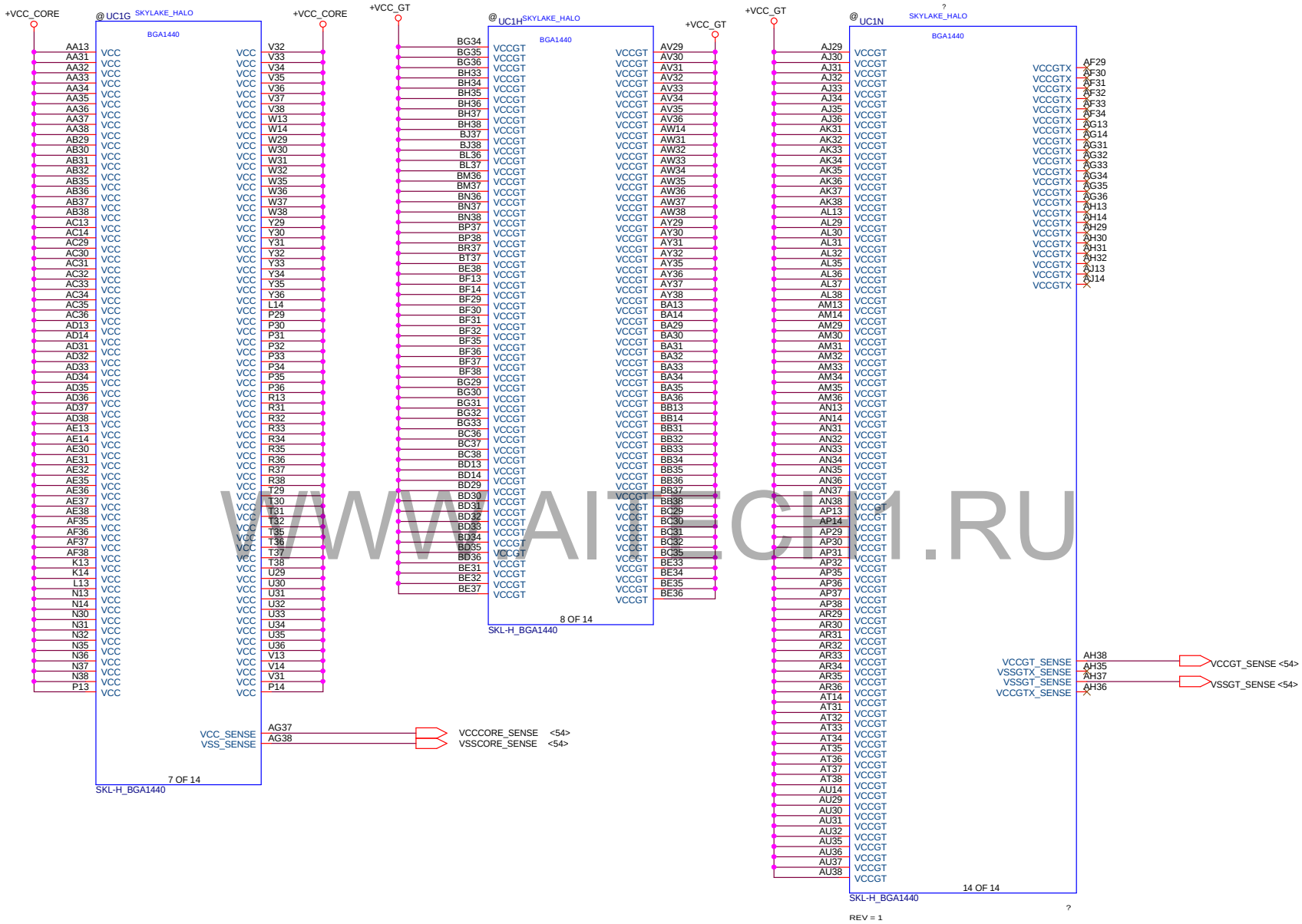

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Title: **VCC/VCCGT**

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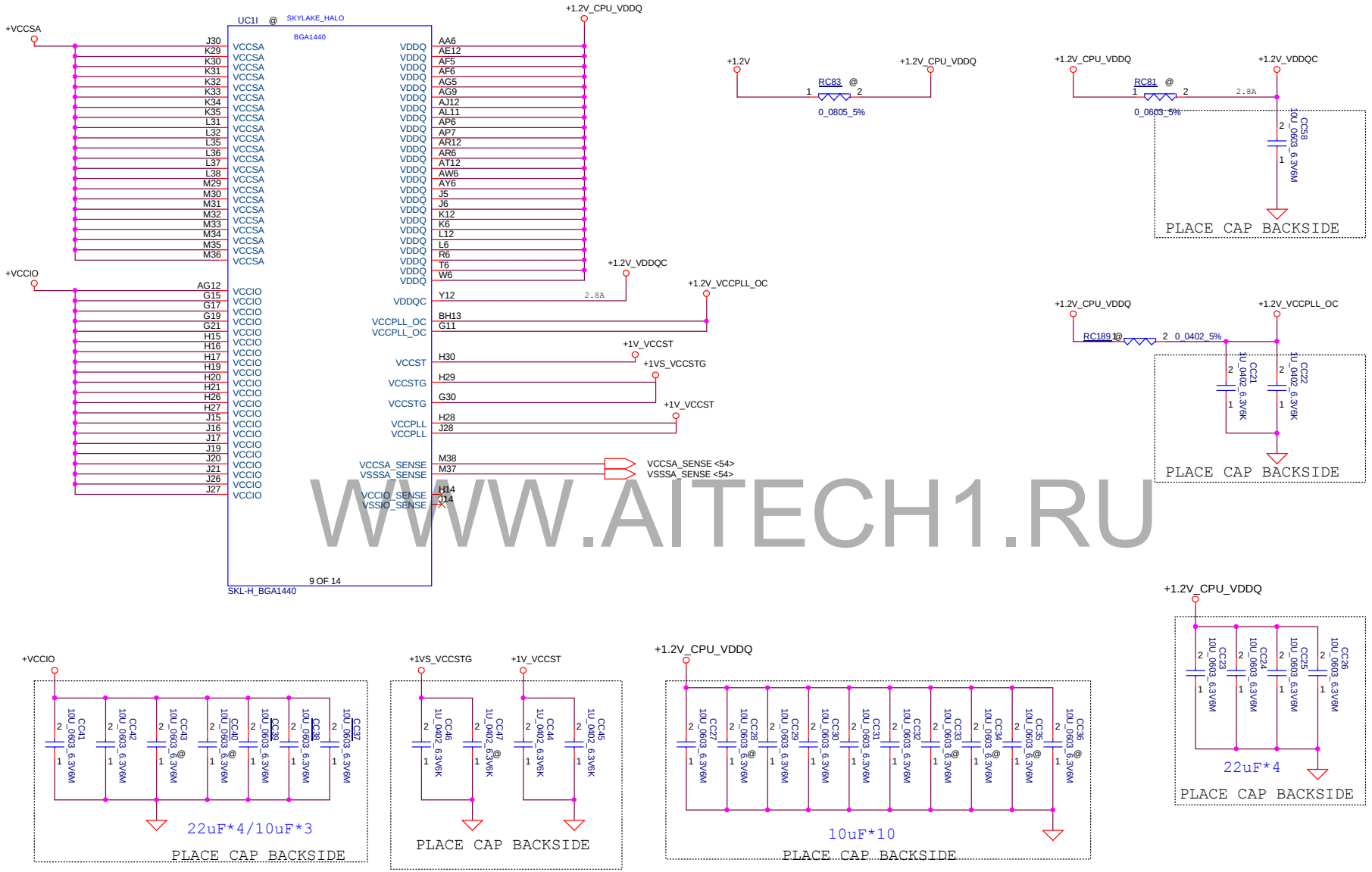

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Title: **VDDQ/VCCSA/VCCIO**

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CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

check GPU PEG

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Skylake H Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BR2	NCTF	Test Point (TP)	Corner BT1
BR1	NCTF	Test Point (TP)	
C1	NCTF	Test Point (TP)	Corner A1
B2	NCTF	Test Point (TP)	
C38	NCTF	Test Point (TP)	Corner A38
B38	NCTF	Test Point (TP)	
BR38	NCTFVSS	Test Point (TP)	Corner BT38
BT36	NCTFVSS	Test Point (TP)	

Refer to *Processor EDS* for more details on NCTF information.

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Title: RSVD,CFG		
Size: Custom	Document Number: LA-C951P	Rev: 1.0
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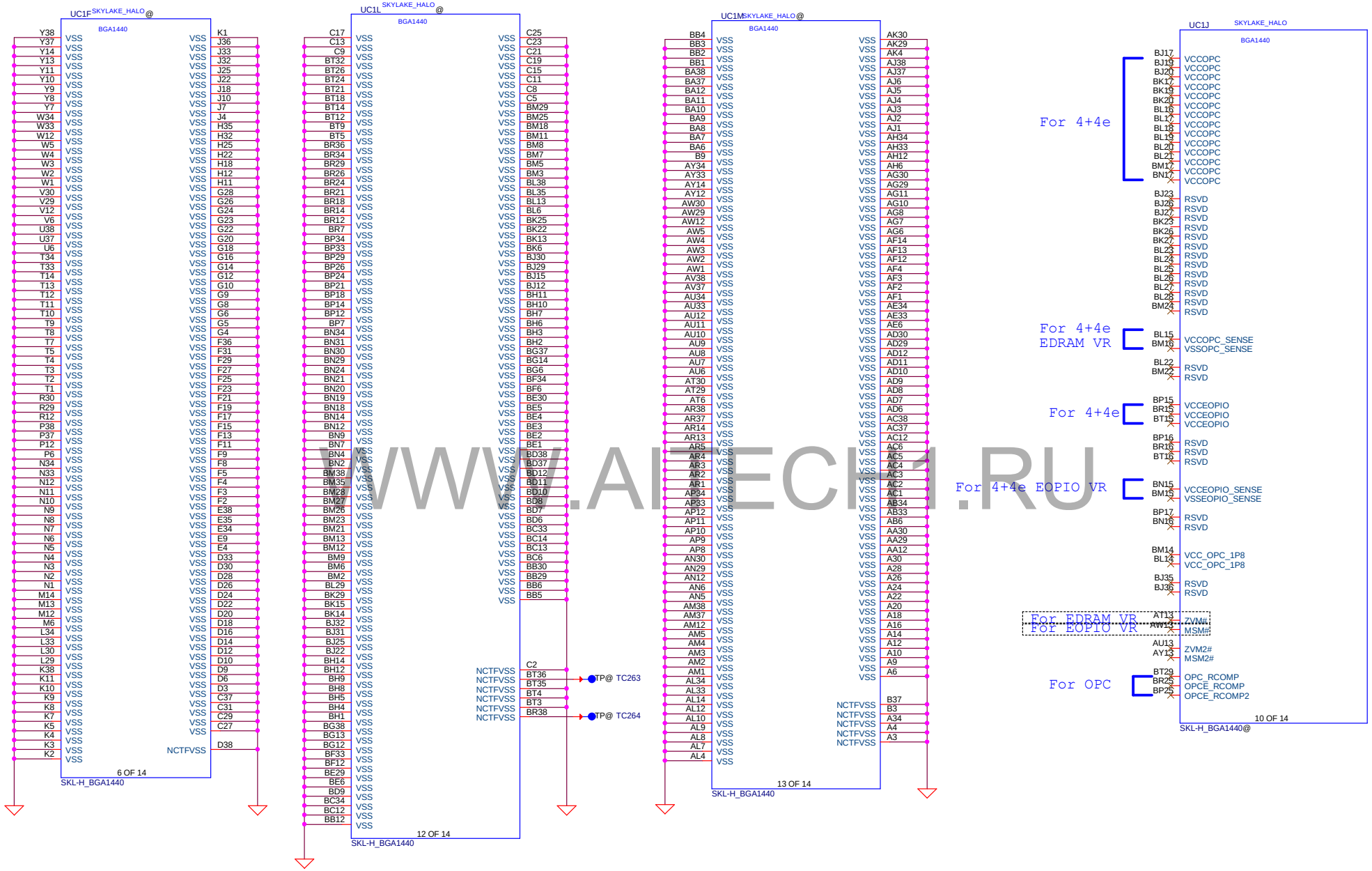

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Title: **VSS/VCCOPC**

Size	Document Number	Rev
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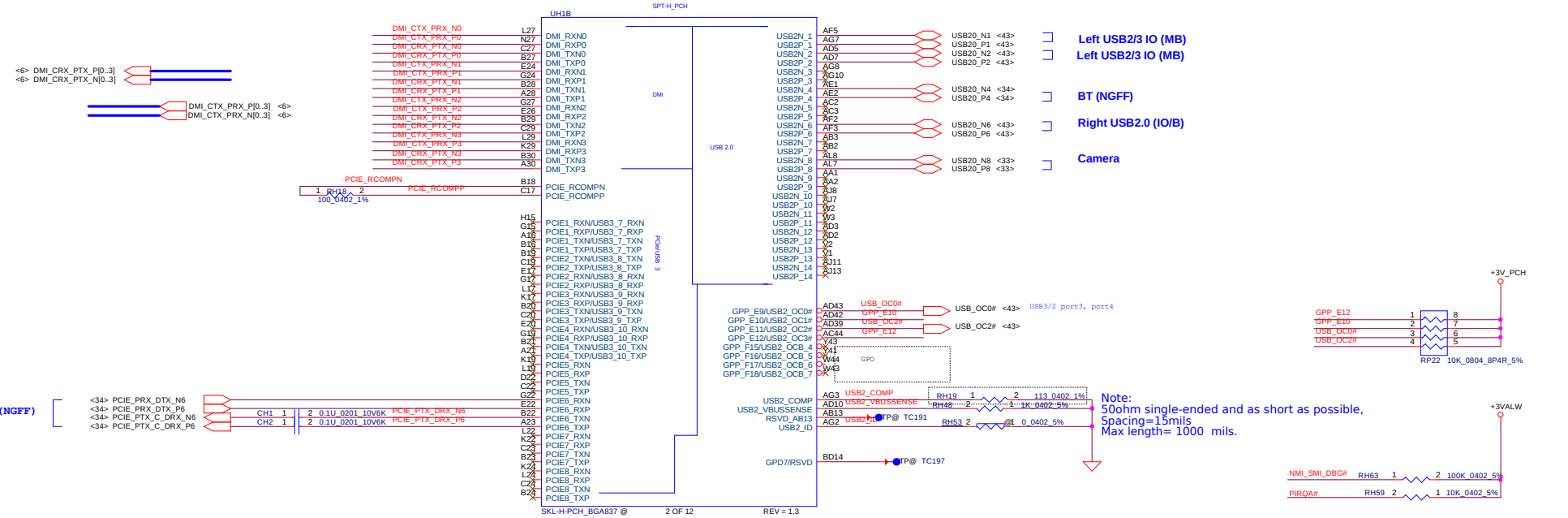

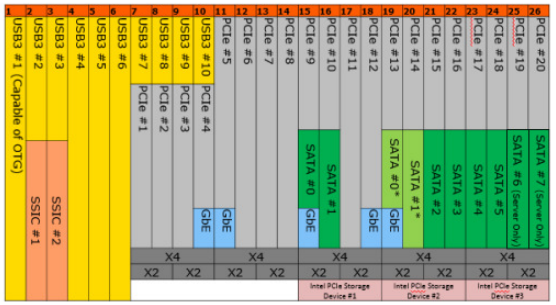

USB2.0

Port	1	2	3	4	5	6	7	8
	Left USB3.0	Left USB3.0		BT (NGFF)		Right USB2.0		Camera

Flexible I/O Capable Ports

HSIO Port	3	4	~~~	12	16	17	18	19	20	21	22
USB 3.0	3 USB3.0_1	4 USB3.0_2									
PCIe				6 WLAN		11 CardReader	12 LAN	13 NGFF(SSD)	14 NGFF(SSD)	15 NGFF(SSD)	16 NGFF(SSD)
SATA					1 HDD(SSD)			0 NGFF(SSD)			

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Compal Electronics, Inc.	
Title	DMI,USB,PCIE,LPC
Size: Custom	Document Number: LA-C951P
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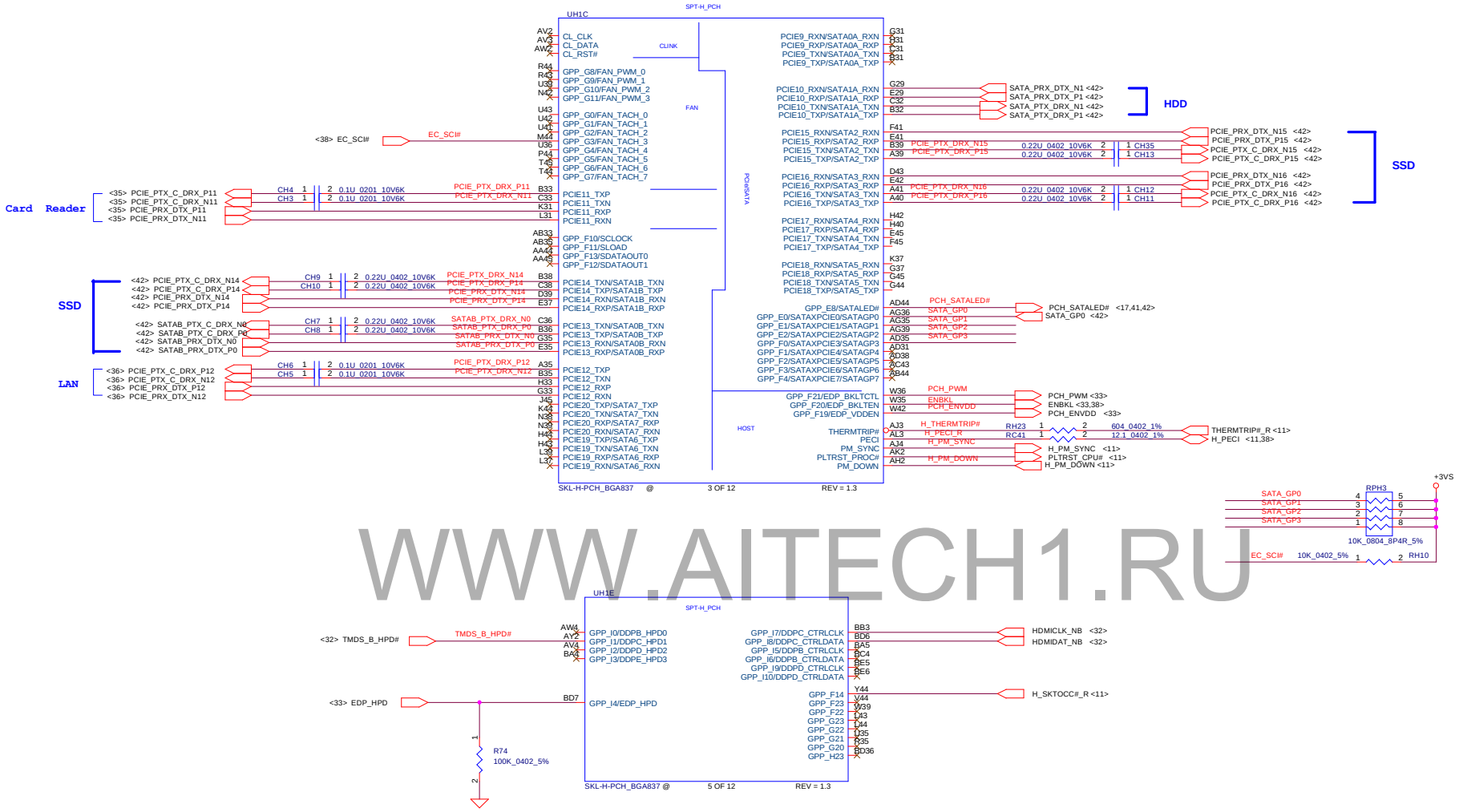

Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
HM170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26)

SKU	15	16	17	18	19	20	21	22	23	24	25	26
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A
H170	PCIe/LAN /SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN /SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe
HM170	PCIe/LAN /SATA0	PCIe/ LAN/ SATA1	PCIe	PCIe/ LAN	PCIe/ LAN/ SATA0	PCIe/ SATA1	PCIe/ SATA	PCIe/ SATA	N/A	N/A	N/A	N/A

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

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Title	SATA,GPIO
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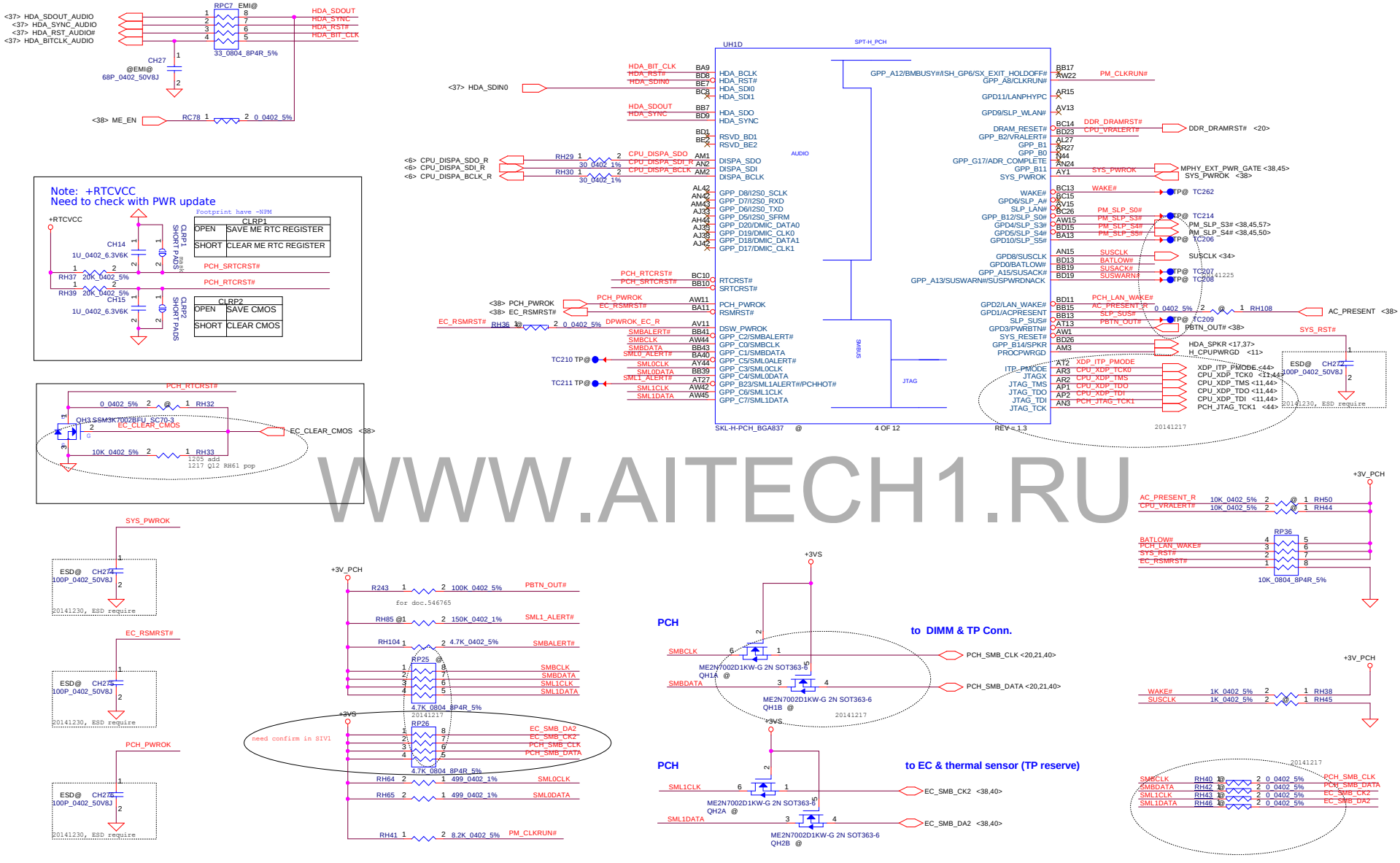

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Title: **SMB,HDA,JTAG**

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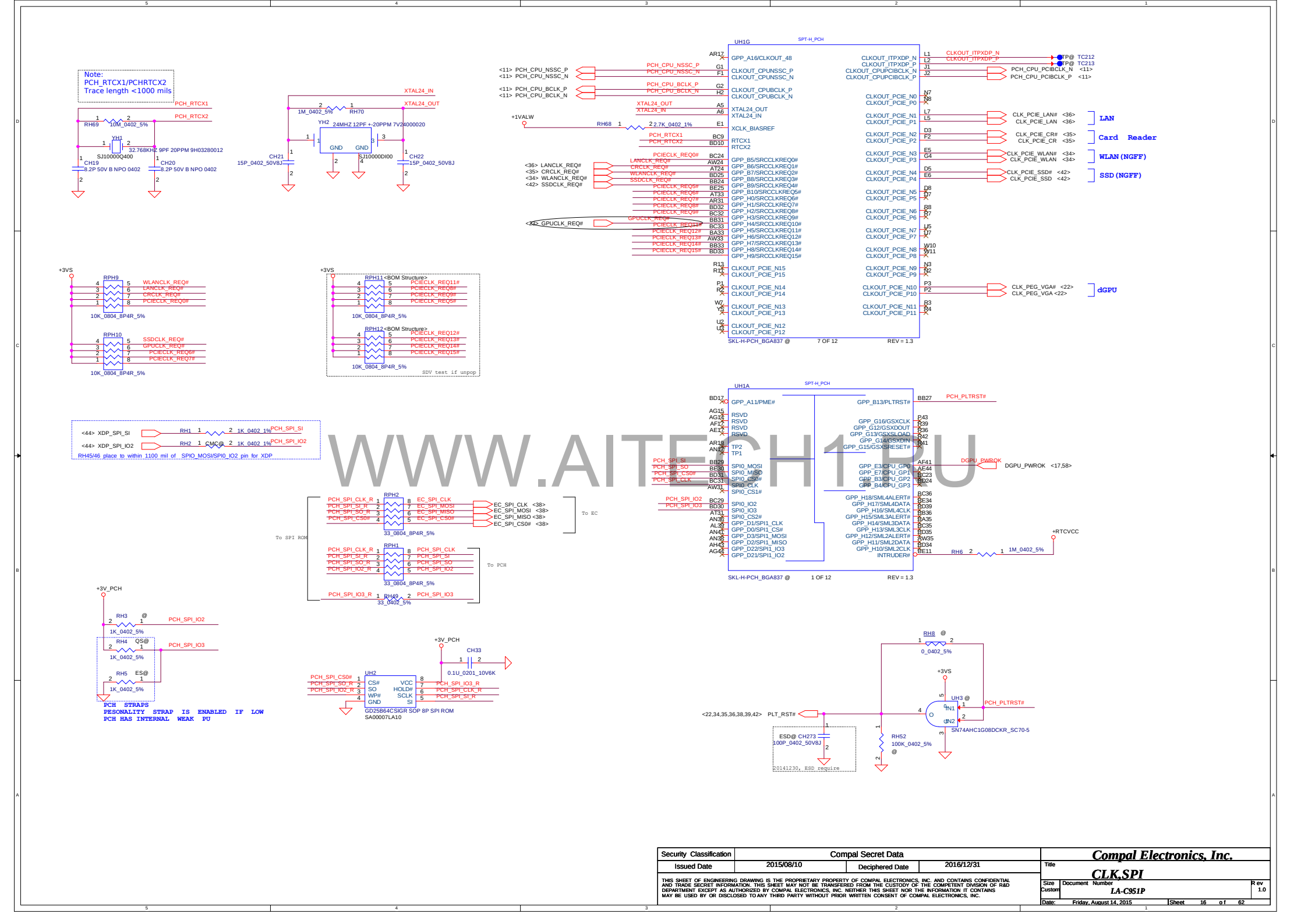

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Compal Electronics, Inc.

Title: **CLK,SPI**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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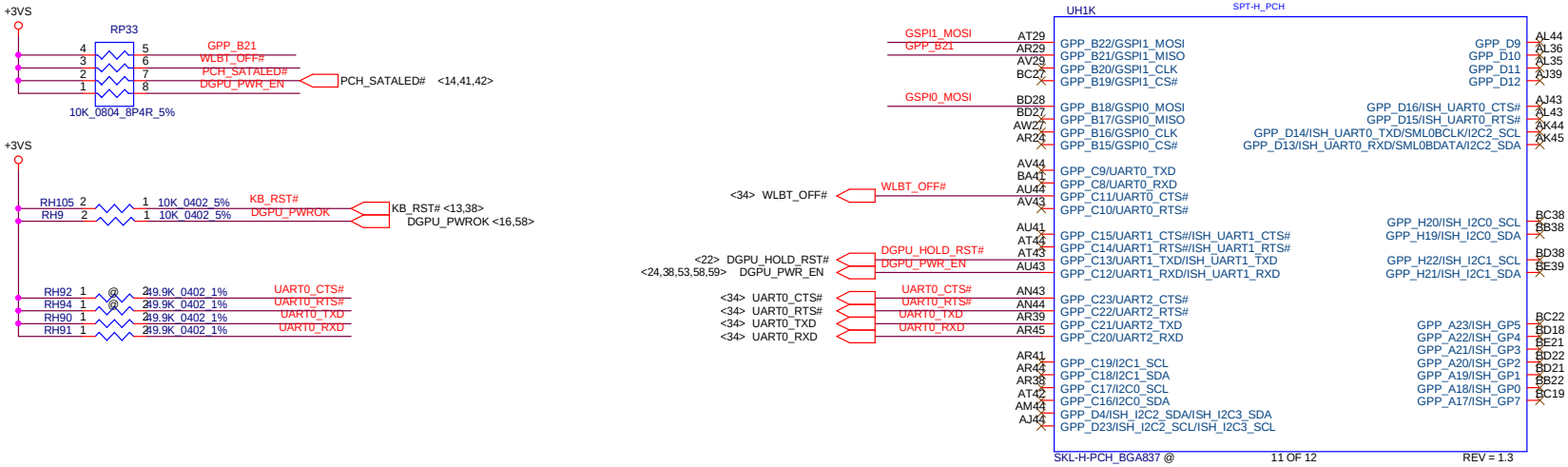


Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> ORB Use

***1 = Enable TOP Swap Mode.**

GSPI0_MOSI (Internal Pull Down):

No Reboot

***0 = Disable No Reboot mode. --> ORB Use**

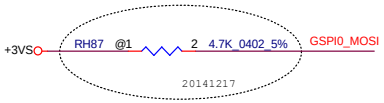
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

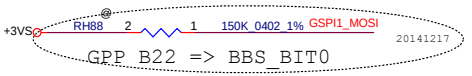
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

***0 = SPI Mode --> ORB Use**

1 = LPC Mode





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Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **I2C,UART,GPIO**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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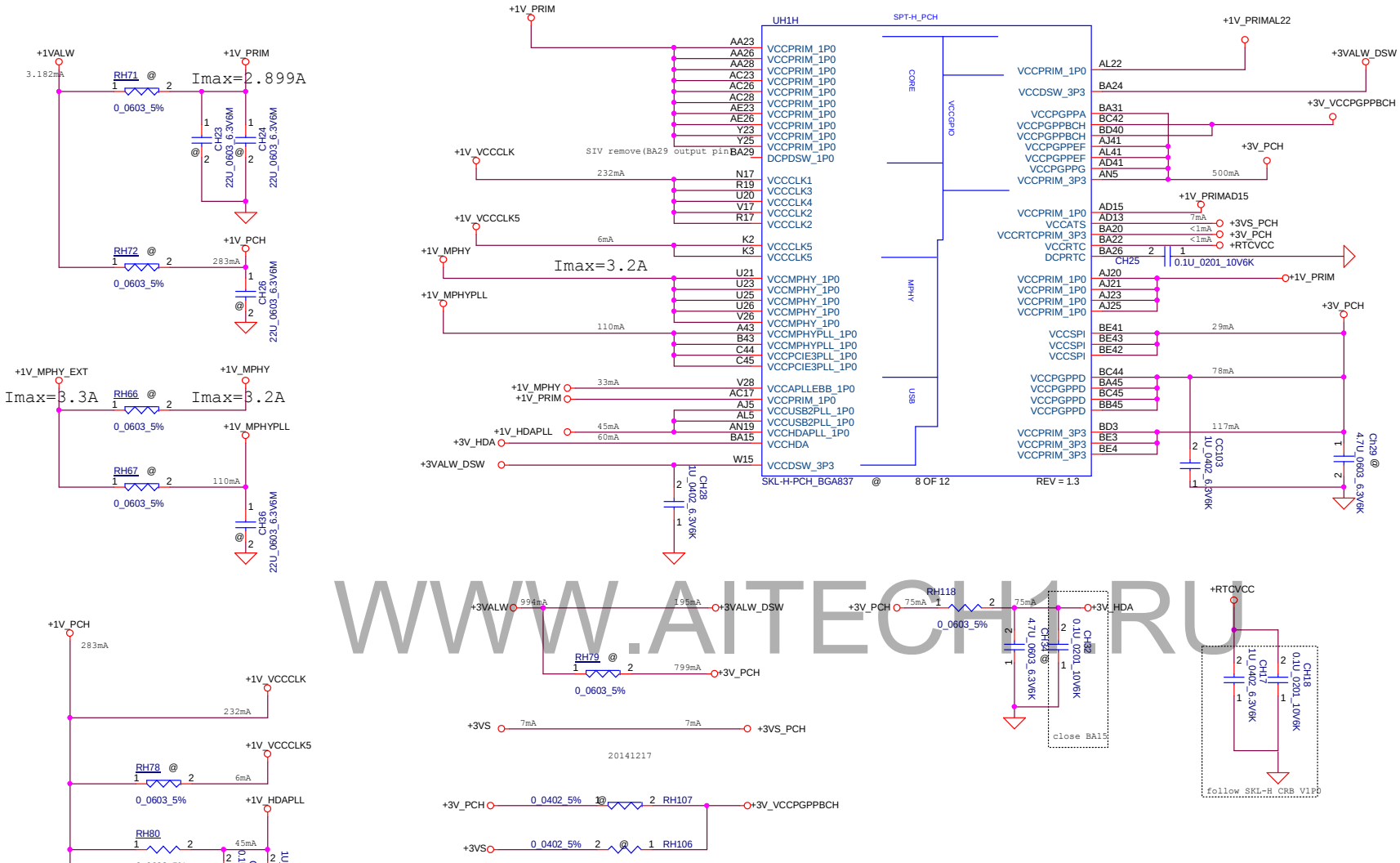

Skylake PCH VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (mA)	Details
700	All HSIO disabled. Assumes DMI x4 Running 100%.
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GbE Port

DMI x 4
Gen3 x 12 (PEGx8+SSDX4)
USB3.0 x 2
Gen2 x 3 (CR+LAN+WLAN)
Sata x 1
Imax=3.2A

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Compal Electronics, Inc.

Title: VCC

Size	Document Number	Rev
Custom	LA-C951P	1.0

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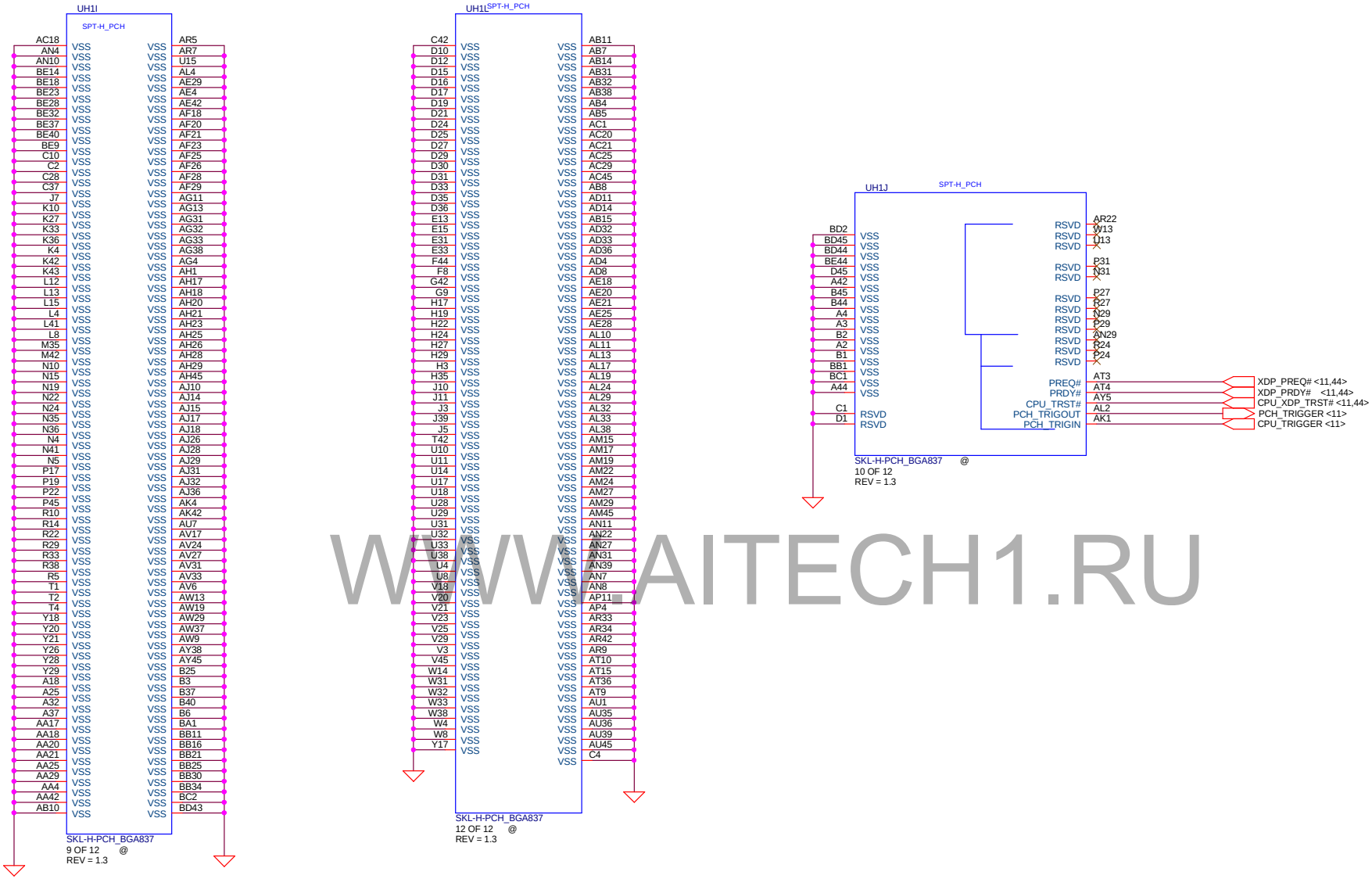

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Title: **VSS,RSVD**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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CHANNEL-A Interleaved Memory

Non-ECC DIMM

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

(4 mm)

REVERSE

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

Place near SODIMM side.

DIMM1 Side

CPU Side

PLACE NEAR TO PIN

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Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	DDRIV DIMM1		
Size	Document Number		Rev
Custom	LA-C951P		1.0
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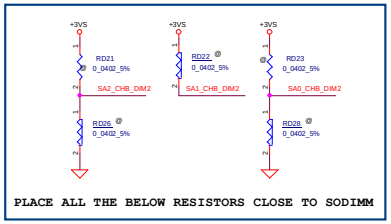
CHANNEL-B Interleaved Memory

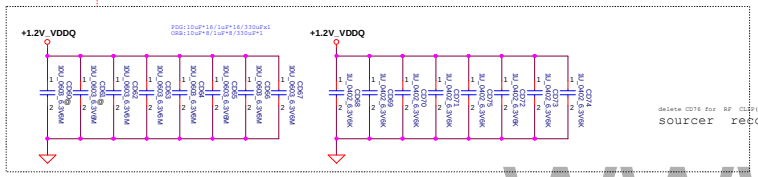
Non-ECC DIMM

BOT (8 mm) REVERSE



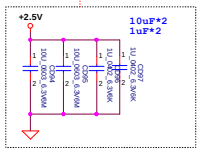
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

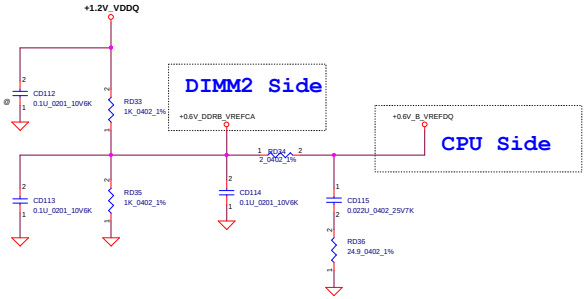
Layout Note:
Place near JDIMM3



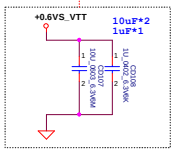
delete CD76 for RF CLK(0616)
sourcer recommend(4/10)

Layout Note:
Place near JDIMM2

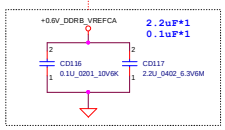


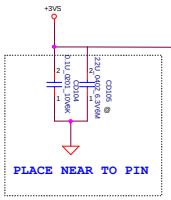


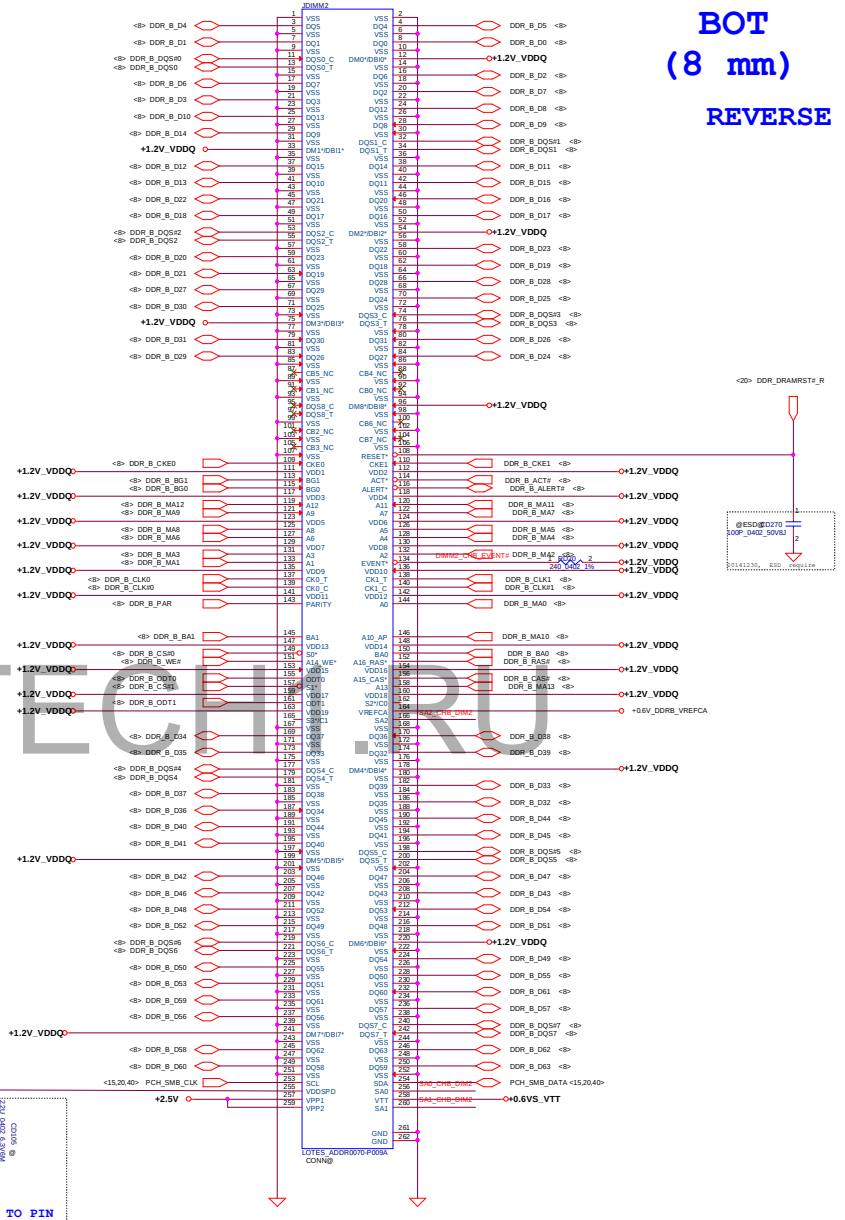
Layout Note:
Place near JDIMM2



Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



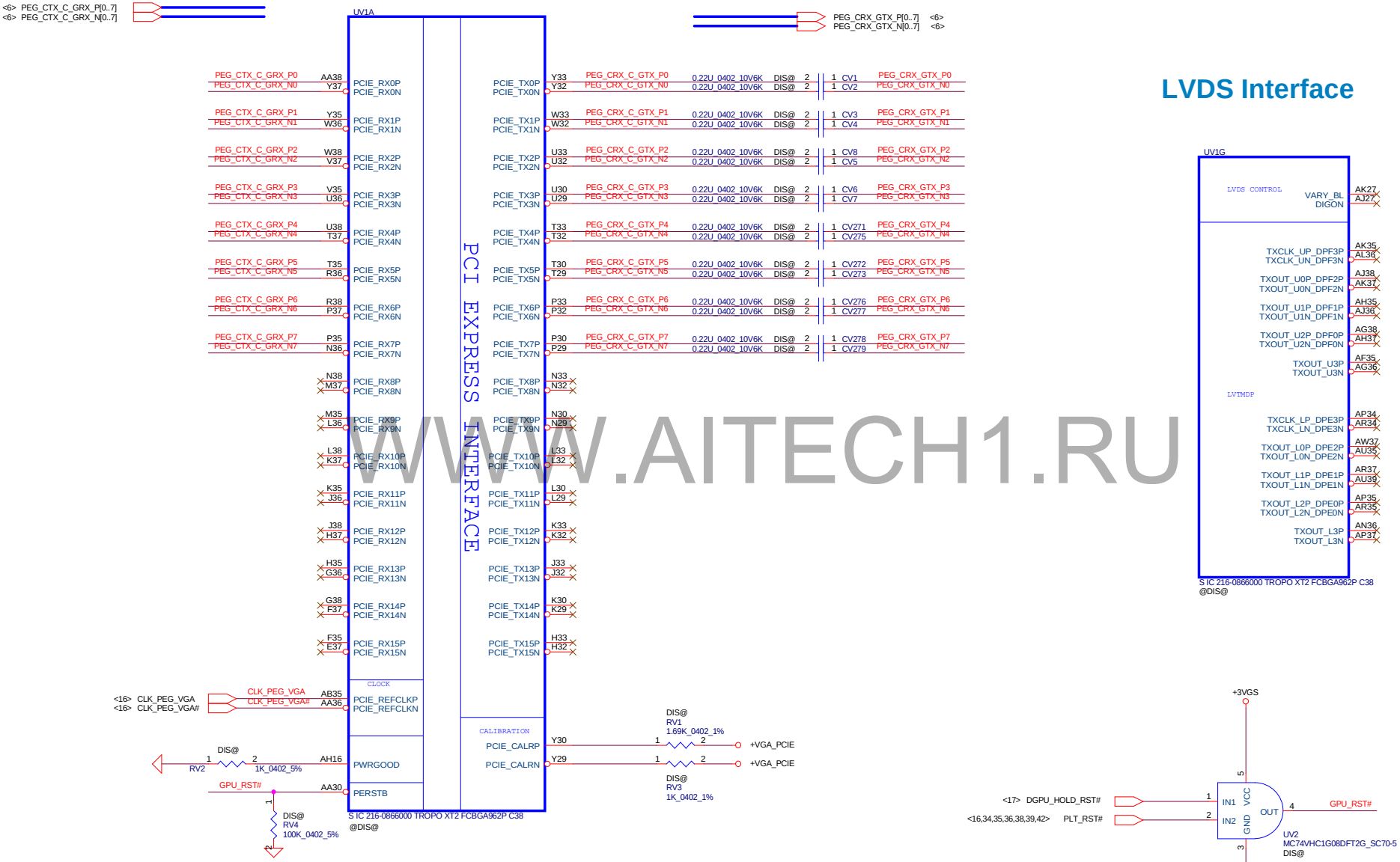




Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	DDRIV DIMM2		
Size	Document Number		Rev
Custom	LA-C951P		1.0
Date: Friday, August 14, 2015	Sheet 21 of 62		

GFX PCIE LANE REVERSAL



LVDS Interface

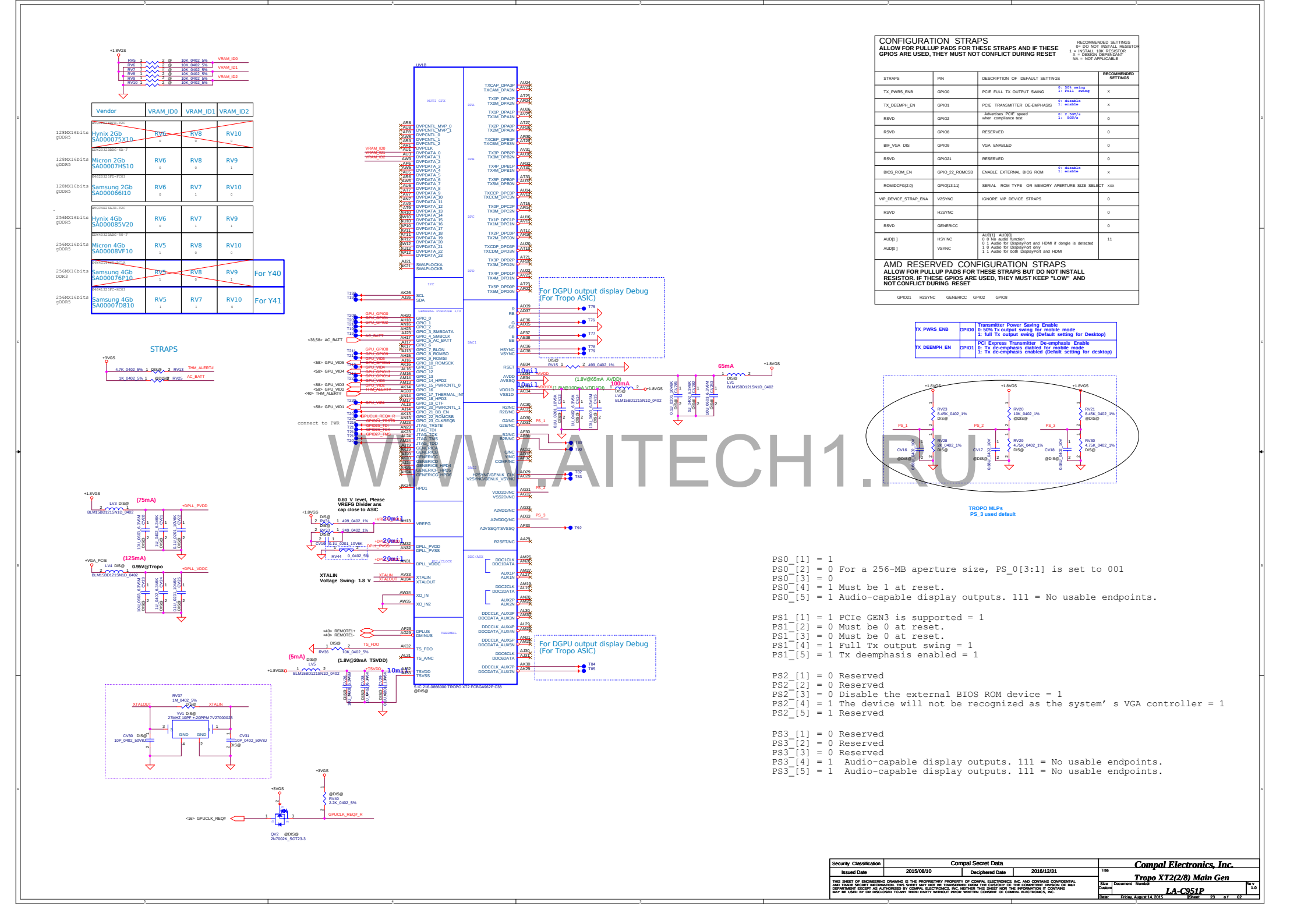
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **Tropo XT2(1/8) PCIE/PWRseq**

Size	Document Number	Rev
Custom	LA-C951P	1.0

Date: Friday, August 14, 2015 Sheet 22 of 62


+1.8VGS
RV5 1 2 @ 10K_0402_5%
RV6 1 2 @ 10K_0402_5%
RV7 1 2 @ 10K_0402_5%
RV8 1 2 @ 10K_0402_5%
RV9 1 2 @ 10K_0402_5%
RV10 1 2 @ 10K_0402_5%
VRAM_ID0
VRAM_ID1
VRAM_ID2
Vendor
VRAM_ID0
VRAM_ID1
VRAM_ID2
128MX16bits gDDR5
Hynix 2Gb SA000075X10
RV6 0
RV8 0
RV10 0
128MX16bits gDDR5
Micron 2Gb SA00007HS10
RV6 0
RV8 0
RV9 1
128MX16bits gDDR5
Samsung 2Gb SA000066I10
RV6 0
RV7 1
RV10 0
256MX16bits gDDR5
Hynix 4Gb SA000085V20
RV6 0
RV7 1
RV9 1
256MX16bits gDDR5
Micron 4Gb SA00008VF10
RV5 1
RV8 0
RV10 0
256MX16bits DDR3
Samsung 4Gb SA000076P10
RV5 1
RV8 0
RV9 1
For Y40
256MX16bits gDDR5
Samsung 4Gb SA00007D810
RV5 1
RV7 1
RV10 0
For Y41
STRAPS
+3VGS
4.7K_0402_5% 1 RV50 2 RV13 THM_ALERT#
1K_0402_5% 1 RV25 2 RV51 AC_BATT
UV1B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
FAN CLOCK
THERMAL
DDC/AUX
TXCAP_DPA3P TXCAM_DPA3N
TX0P_DPA2P TX0M_DPA2N
TX1P_DPA1P TX1M_DPA1N
TX2P_DPA0P TX2M_DPA0N
TXCBP_DPB3P TXCBM_DPB3N
TX3P_DPB2P TX3M_DPB2N
TX4P_DPB1P TX4M_DPB1N
TX5P_DPB0P TX5M_DPB0N
TXCCP_DPC3P TXCCM_DPC3N
TX0P_DPC2P TX0M_DPC2N
TX1P_DPC1P TX1M_DPC1N
TX2P_DPC0P TX2M_DPC0N
TXCDP_DPD3P TXCDM_DPD3N
TX3P_DPD2P TX3M_DPD2N
TX4P_DPD1P TX4M_DPD1N
TX5P_DPD0P TX5M_DPD0N
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
SWAPLOCKA
SWAPLOCKB
SCL
SDA
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG_HPD6
HPD1
VREFG
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT
XO_IN
XO_IN2
DPLUS
DMINUS
TS_FDO
TS_AINC
TSVDD
TSVSS
SIC 216-0866000 TROPO XT2 FCBGA962P C38 @DIS@
For DGPU output display Debug (For Tropo ASIC)
For DGPU output display Debug (For Tropo ASIC)
connect to PWR
0.60 V level, Please VREFG Divider ans cap close to ASIC
XTALIN Voltage Swing: 1.8 V
(1.8V@20mA TSVDD)
(1.8V@65mA AVDD)
(1.8V@100mA VDDIDI)
65mA
100mA
10mil
20mil
(75mA)
(125mA)
(5mA)
0.95V@Tropo
BLM15BD121SN1D_0402
YV1 DIS@ 27MHZ 10PF +-20PPM 7V27000020
QV2 @DIS@ 2N7002K_SOT23-3
GPUCLK_REQ#_R
<16> GPUCLK_REQ#
<38,58> AC_BATT
<58> GPU_VID5
<58> GPU_VID4
<58> GPU_VID3
<58> GPU_VID2
<40> THM_ALERT#
<58> GPU_VID1
<40> REMOTE1+
<40> REMOTE1-
TS_FDO
10K_0402_5%
RV36
RV37 1M_0402_5%
CV30 DIS@ 10P_0402_50V8J
CV31 DIS@ 10P_0402_50V8J
RV40 2.2K_0402_5%
@DIS@
PS_1
PS_2
PS_3
TROPO MLPs
PS_3 used default
RV23 8.45K_0402_1%
RV20 10K_0402_1%
RV21 8.45K_0402_1%
RV28 8K_0402_1%
RV29 4.75K_0402_1%
RV30 4.75K_0402_1%
CV16
CV17
CV18
PS0_[1] = 1
PS0_[2] = 0 For a 256-MB aperture size, PS_0[3:1] is set to 001
PS0_[3] = 0
PS0_[4] = 1 Must be 1 at reset.
PS0_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS1_[1] = 1 PCIe GEN3 is supported = 1
PS1_[2] = 0 Must be 0 at reset.
PS1_[3] = 0 Must be 0 at reset.
PS1_[4] = 1 Full Tx output swing = 1
PS1_[5] = 1 Tx deemphasis enabled = 1
PS2_[1] = 0 Reserved
PS2_[2] = 0 Reserved
PS2_[3] = 0 Disable the external BIOS ROM device = 1
PS2_[4] = 1 The device will not be recognized as the system' s VGA controller = 1
PS2_[5] = 1 Reserved
PS3_[1] = 0 Reserved
PS3_[2] = 0 Reserved
PS3_[3] = 0 Reserved
PS3_[4] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS3_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.
CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS
TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing | x
TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable | x
RSVD | GPIO2 | Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s | 0
RSVD | GPIO8 | RESERVED | 0
BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0
RSVD | GPIO21 | RESERVED | 0
BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM 0: disable 1: enable | x
ROMIDCFG[2:0] | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | xxx
VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0
RSVD | H2SYNC | | 0
RSVD | GENERICC | | 0
AUD[1:] AUD[0:] | HSY NC VSYNC | AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI | 11
AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET
GPIO21 H2SYNC GENERICC GPIO2 GPIO8
TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalit setting for desktop)
WWW.AITECH1.RU
Security Classification | Compal Secret Data
Issued Date | 2015/08/10 | Deciphered Date | 2016/12/31
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Compal Electronics, Inc.
Title: Tropo XT2(2/8) Main Gen
Size: Custom | Document Number: LA-C951P | Rev: 1.0
Date: Friday, August 14, 2015 | Sheet 23 of 62

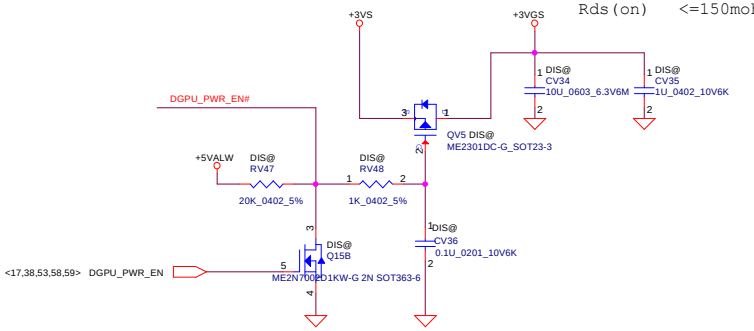
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

Note:

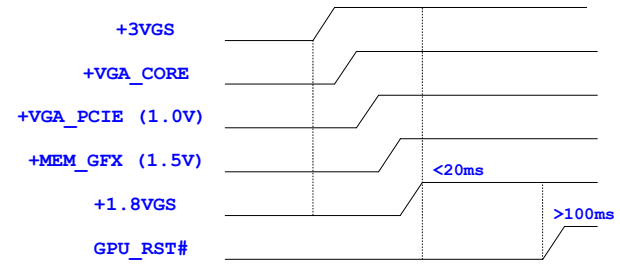
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

+3VS TO +3VGS

ME2301DC
Rds(on) <=110mohm@Vgs=-4.5
Rds(on) <=150mohm@Vgs=-2.5

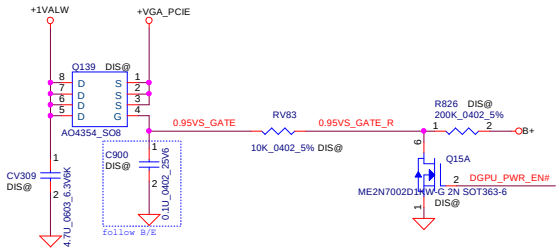


Power seguence of Tropo XT2



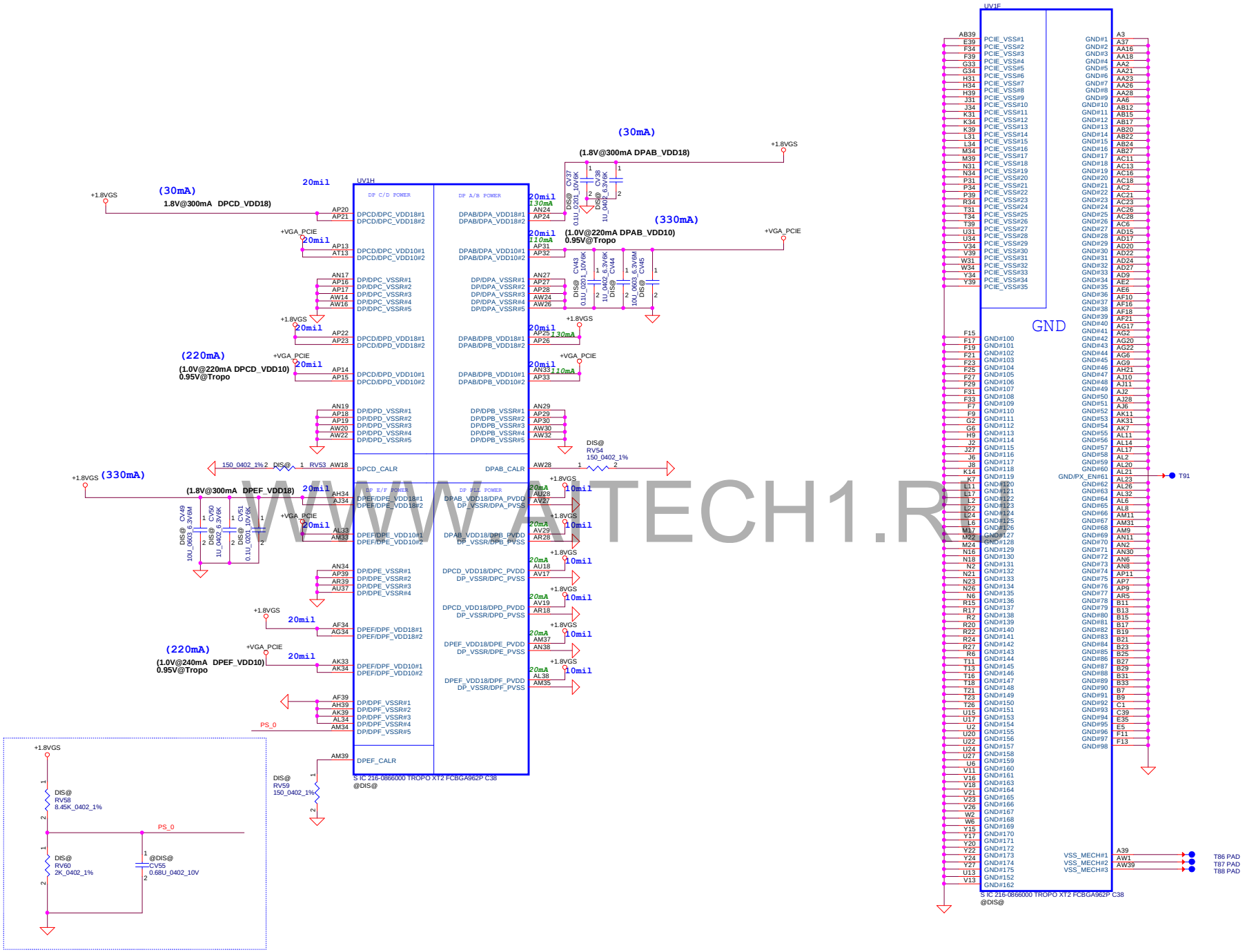
+1VALW to +VGA_PCIE

AO4354
Rds(on) <=5.3mohm@Vgs=4.5
Rds(on) <=3.7mohm@Vgs=10



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: Tropo XT2(3/8) DC/DC POWER			
Size: Custom	Document Number: LA-C951P		Rev: 1.0
Date: Friday, August 14, 2015	Sheet 24 of 62		



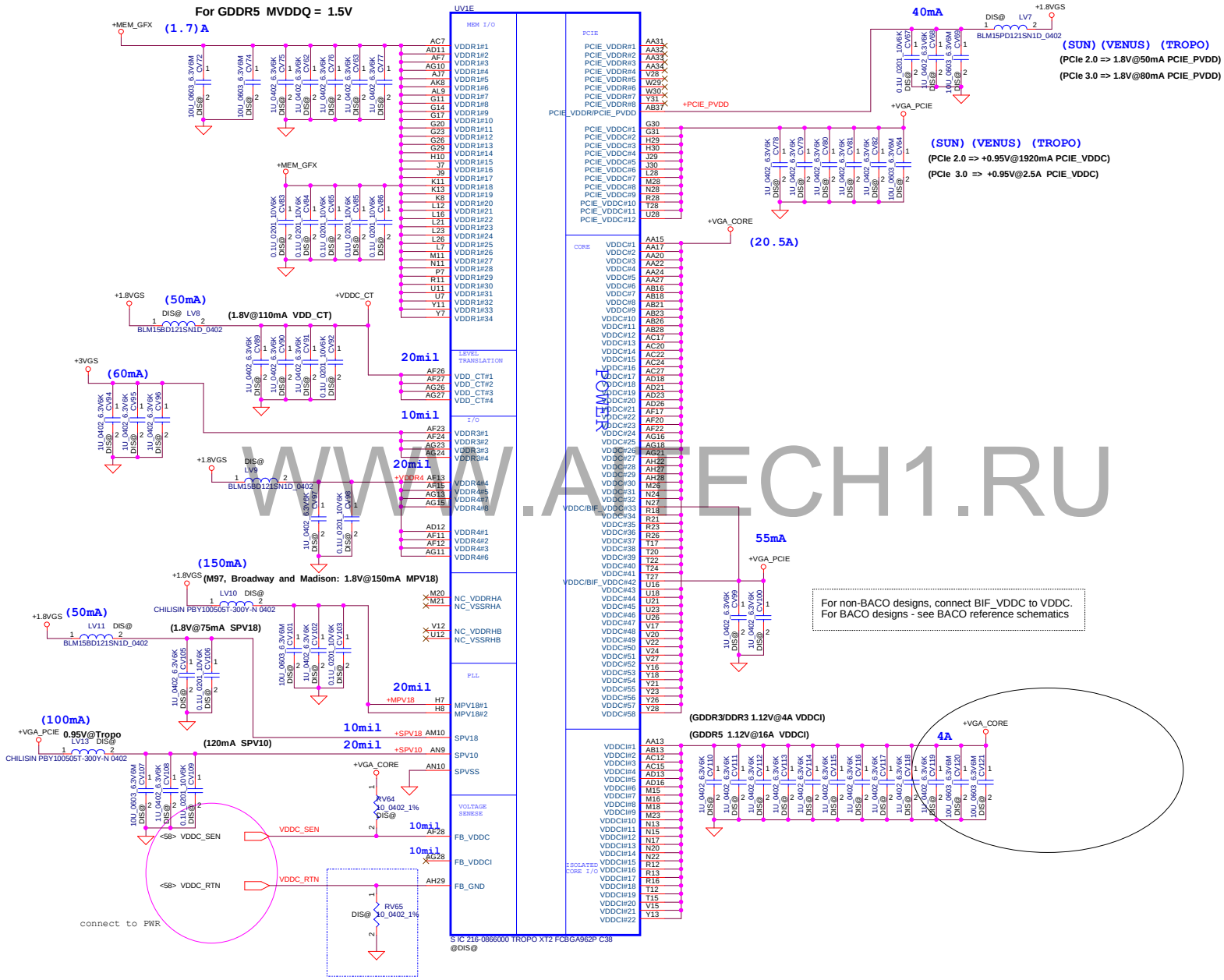
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **Tropo XT2(4/8)DPX Power/GND**

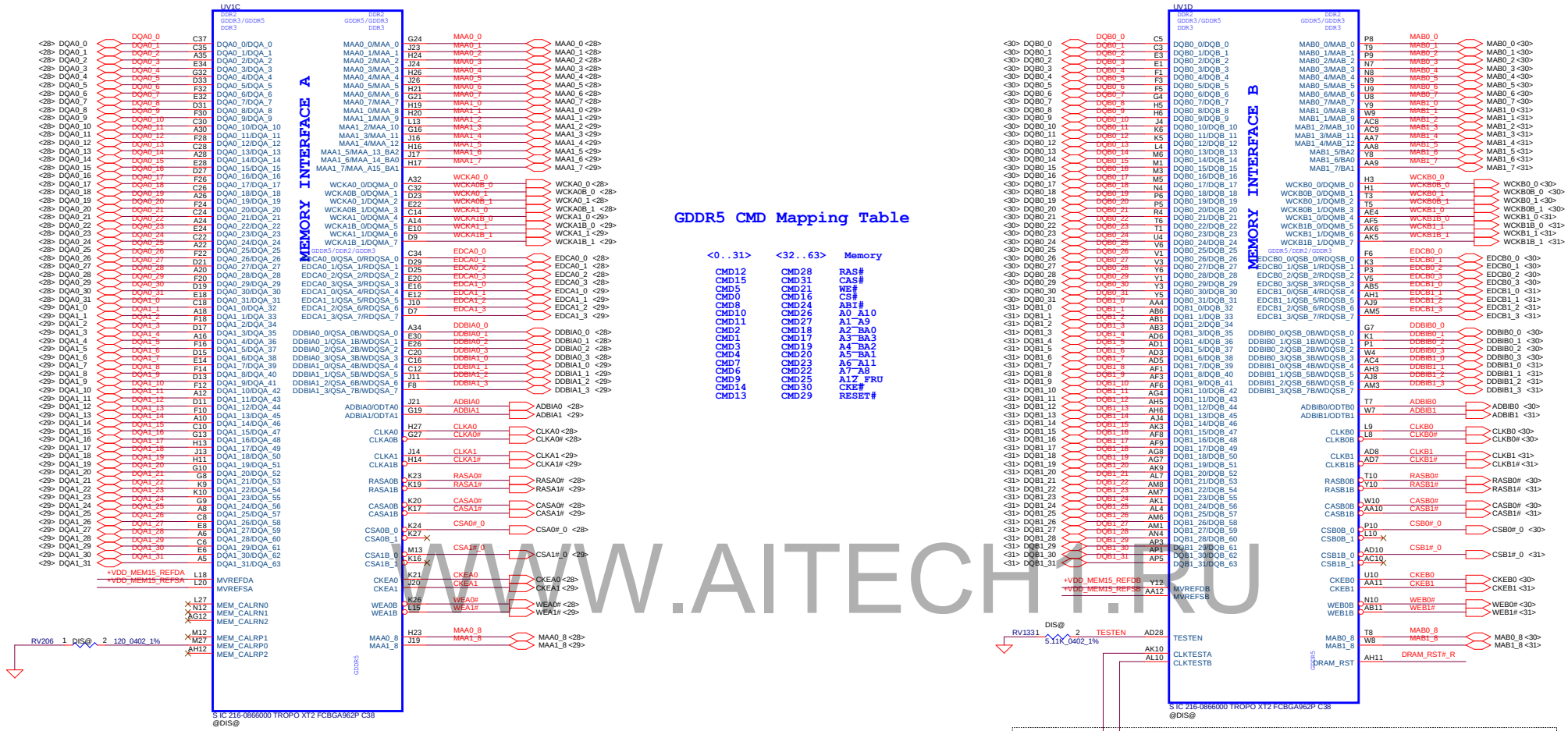
Size: Custom | Document Number: **LA-C951P** | Rev: 1.0

Date: Friday, August 14, 2015 | Sheet 25 of 62



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: Tropo XT2(5/8) Power			
Size: Custom	Document Number: LA-C951P		Rev: 1.0
Date: Friday, August 14, 2015	Sheet 26 of 62		

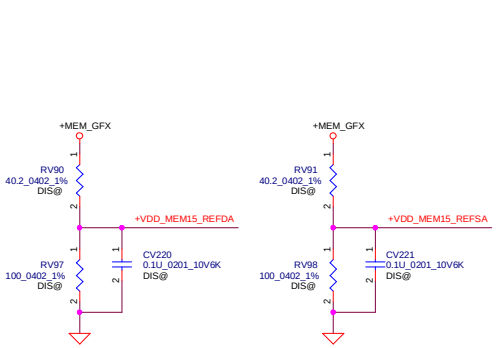


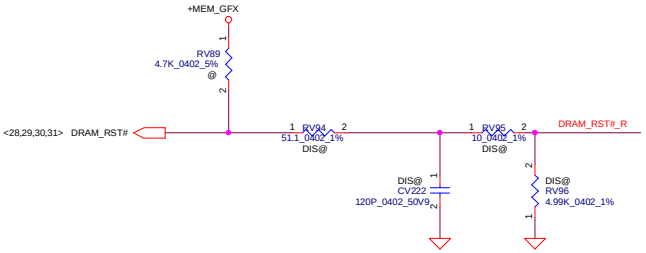
GDDR5 CMD Mapping Table

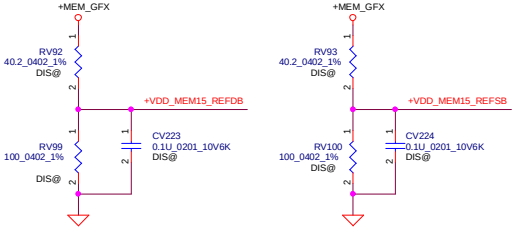
<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A1Z_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

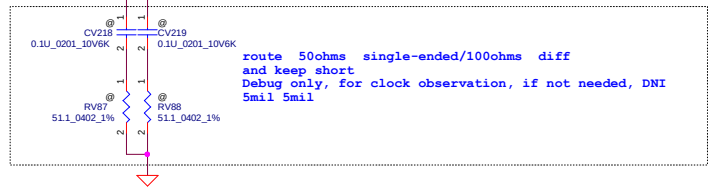
This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil 5mil









Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

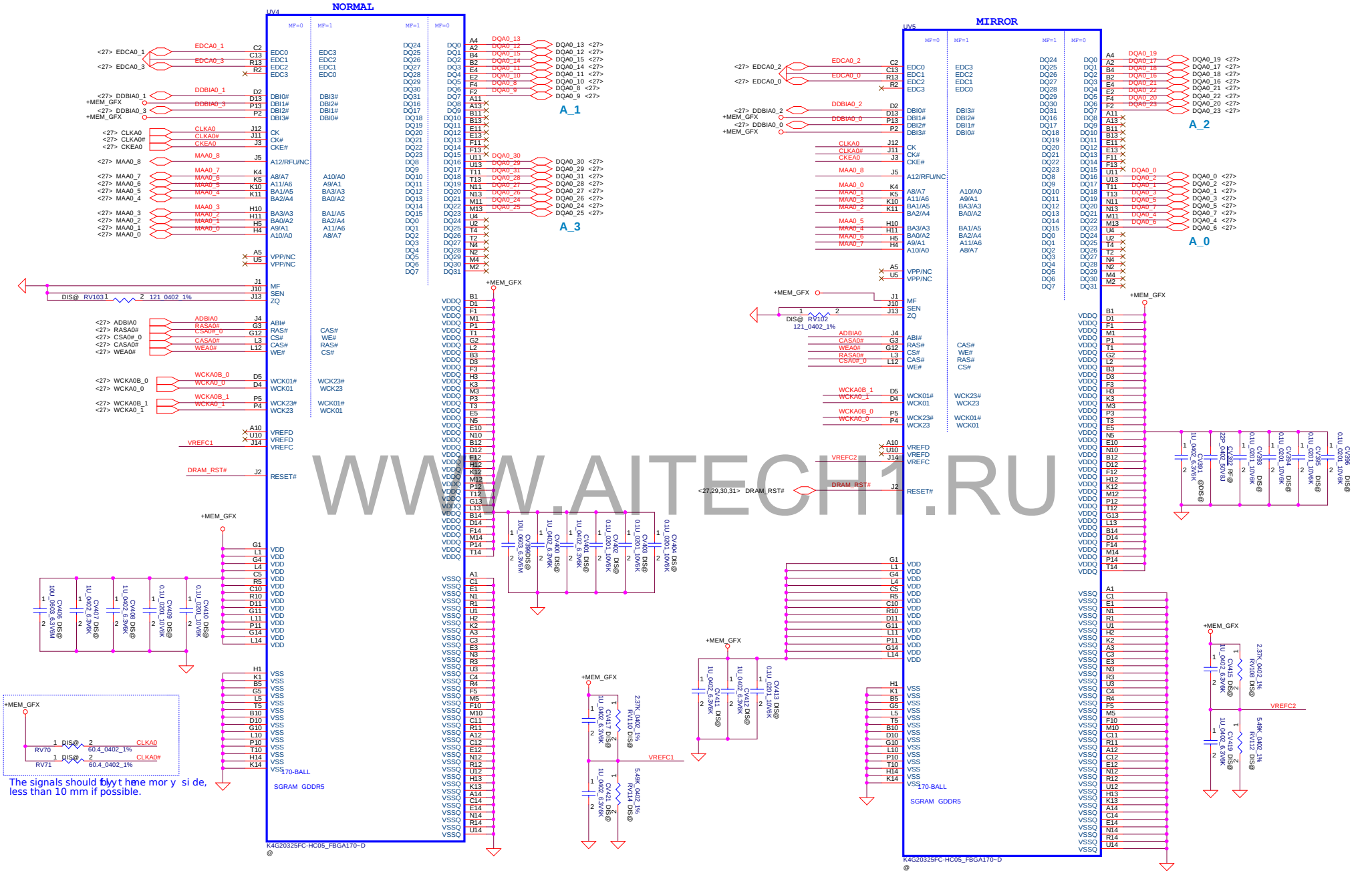
Title: Tropo XT2(6/8)MEM Interface

Size	Document Number	Rev
	LA-C951P	1.0

Date: Friday, August 14, 2015 | Sheet 27 of 62

Memory Partition A - Lower 16 bits

64X32 GDDR5



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

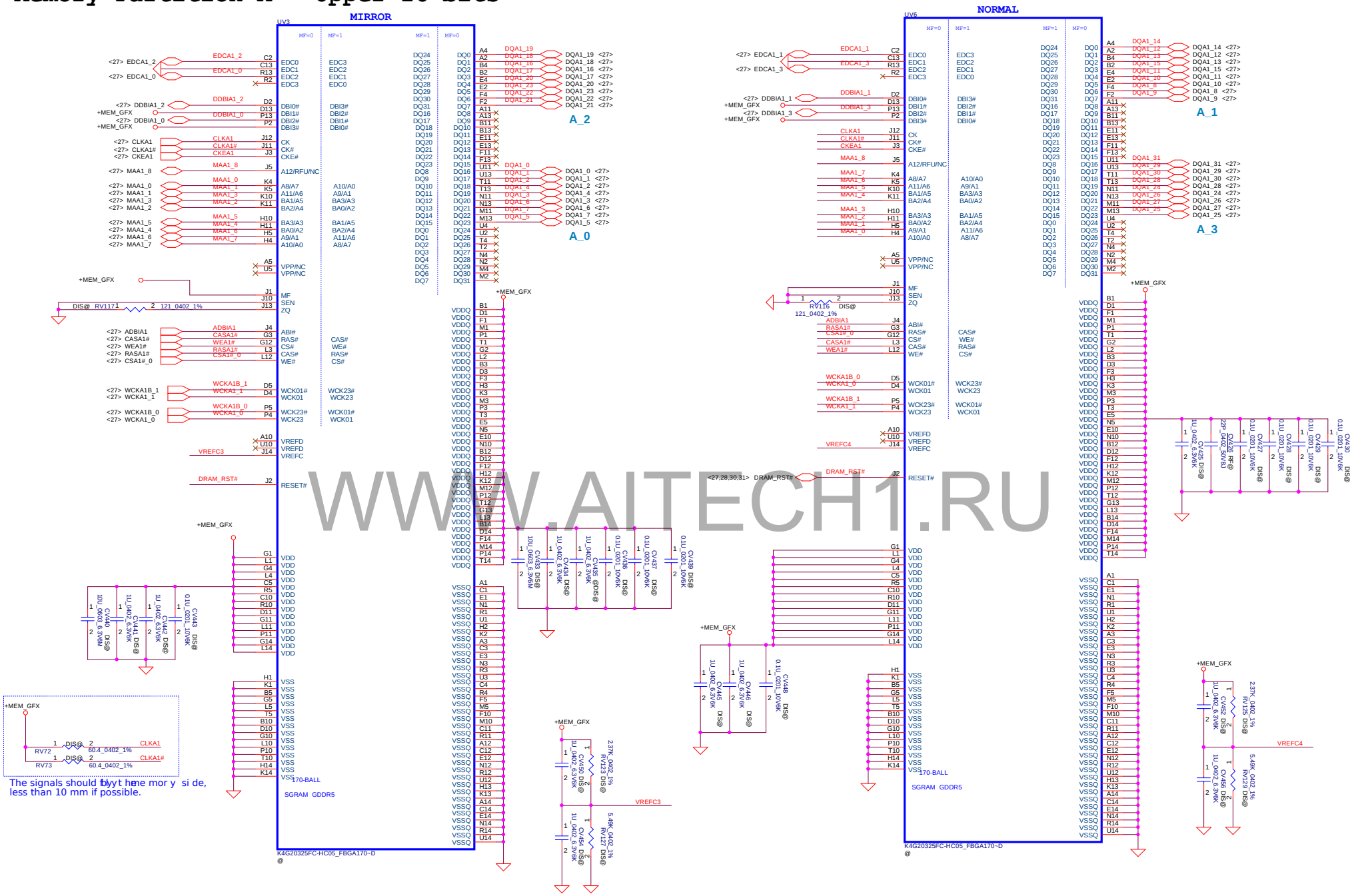
Compal Electronics, Inc.

Title: VRAM_A Lower_UV14,UV15

Size	Document Number	Rev
	LA-C951P	1.0

Date: Friday, August 14, 2015 Sheet 28 of 62

Memory Partition A - Upper 16 bits



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

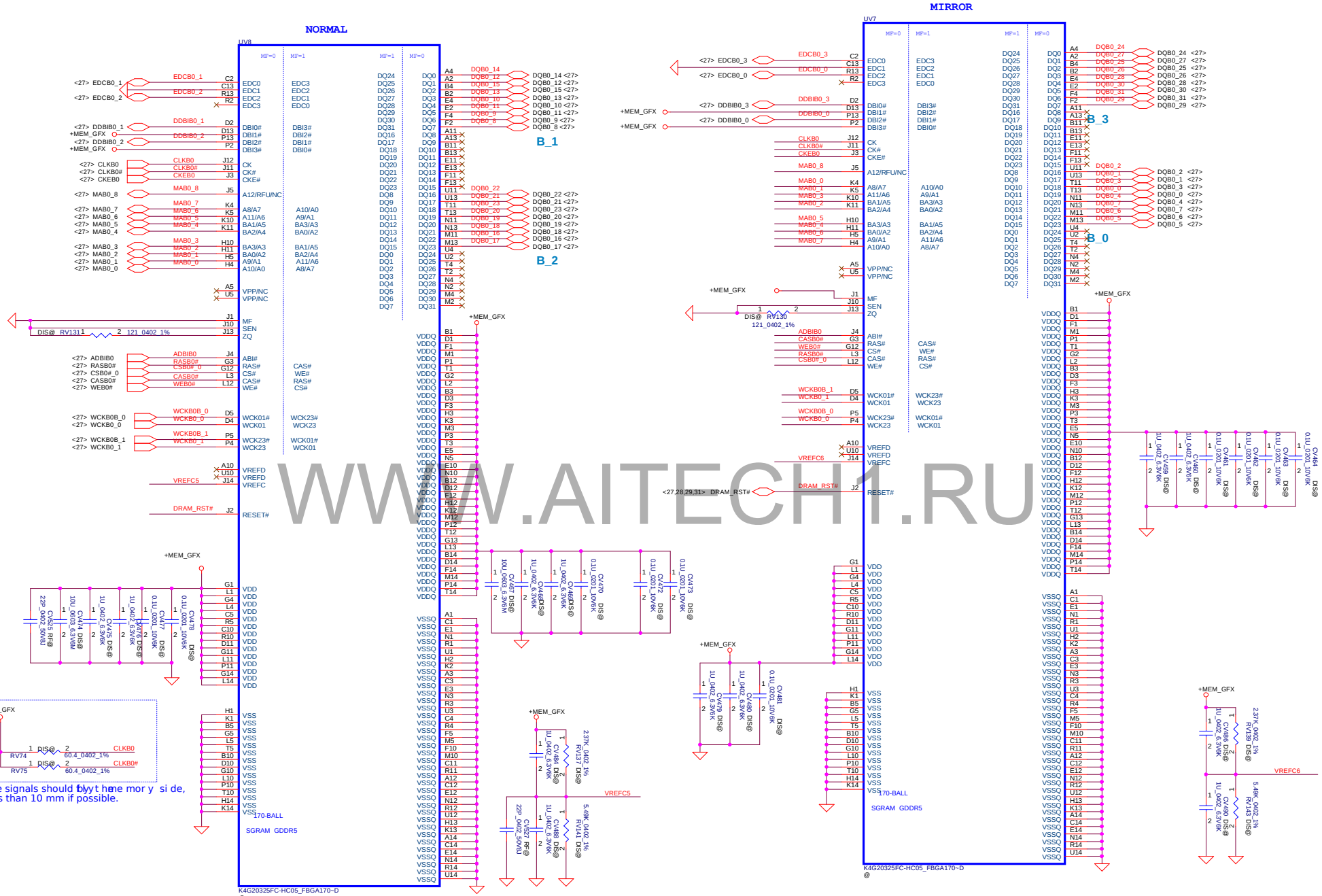
Compal Electronics, Inc.

Title: VRAM_A Upper_UV16,UV17

Size	Document Number	Rev
	LA-C951P	1.0

Date: Friday, August 14, 2015 | Sheet 29 of 62

Memory Partition B - Lower 16 bits



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	VRAM_B Lower_UV18,UV19
Size	Document Number: LA-C951P
Rev	1.0
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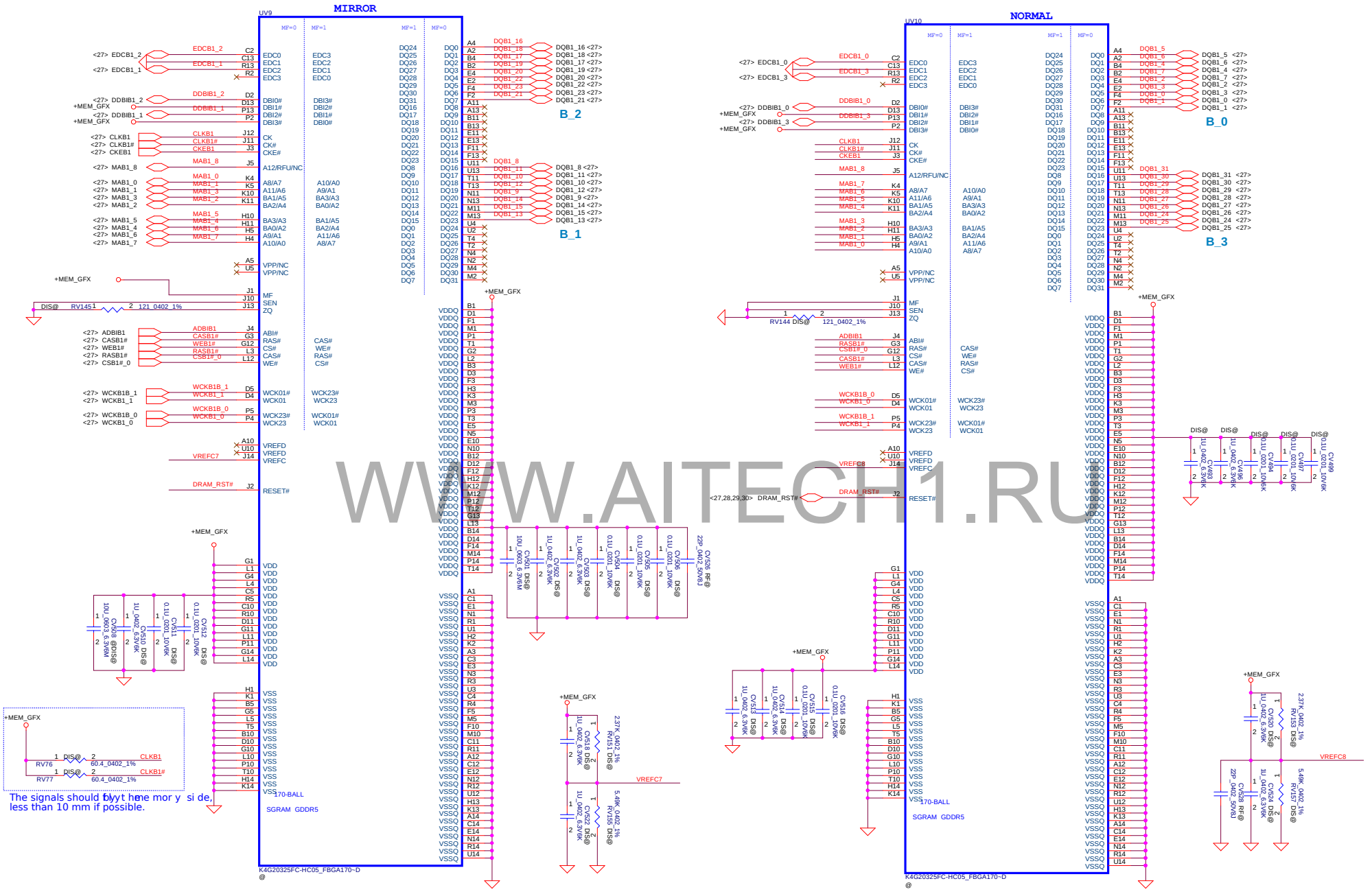
Memory Partition B - Upper 16 bits



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: VRAM_B Lower_UV20,UV21

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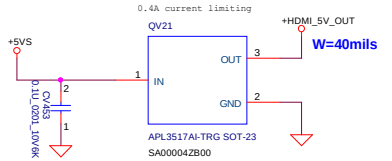
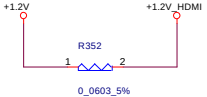
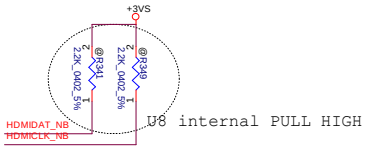
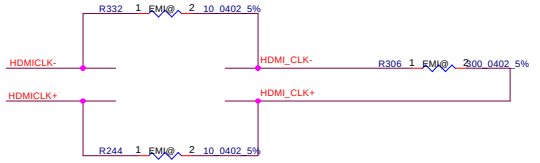
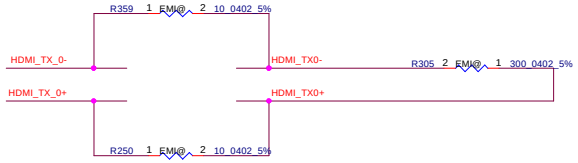
HDMI Active Level Shifter for 4K2K, @2.97Gb/s

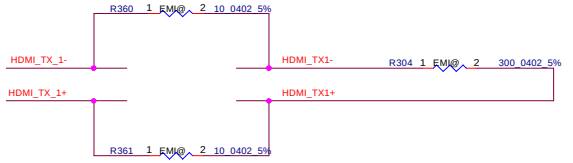


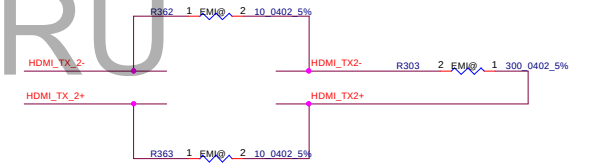


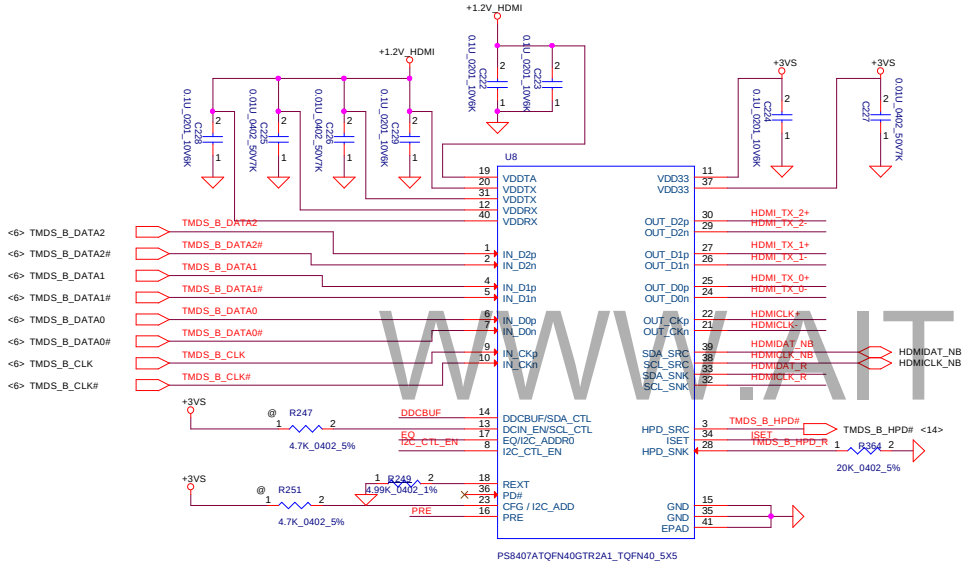


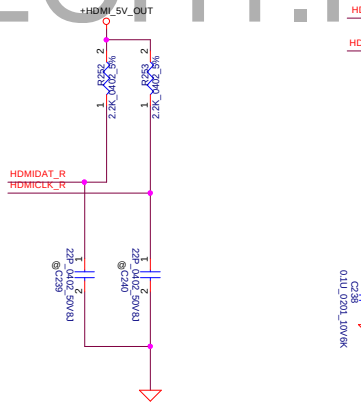


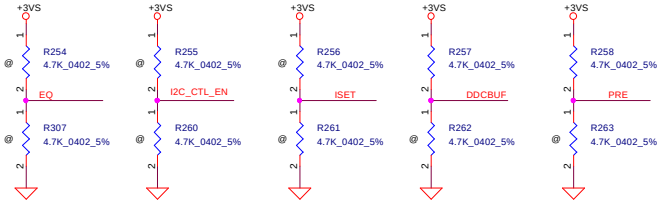


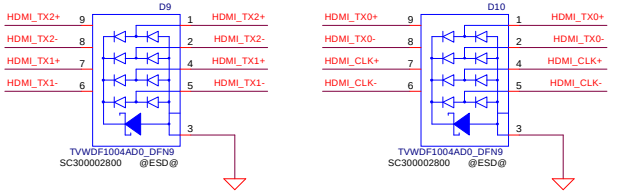


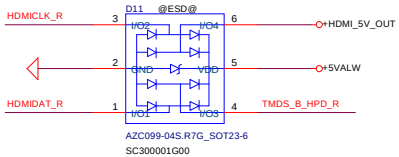


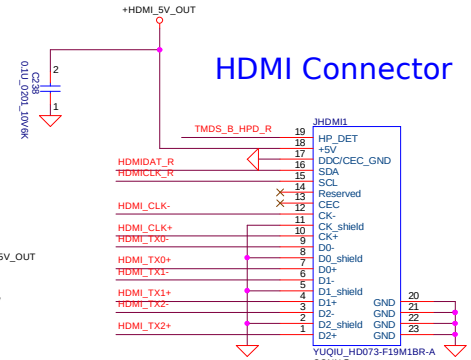












Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **HDMI Level shifter**

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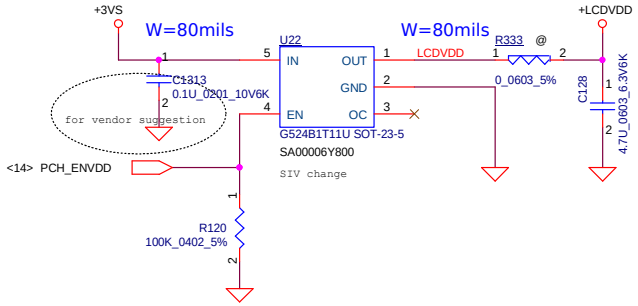
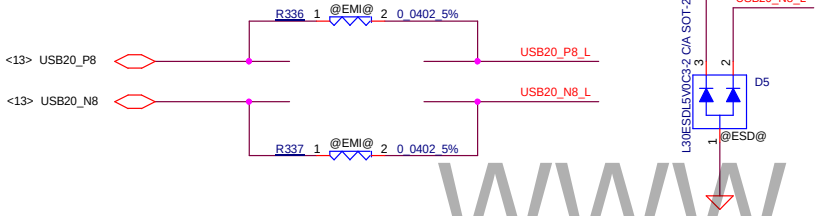
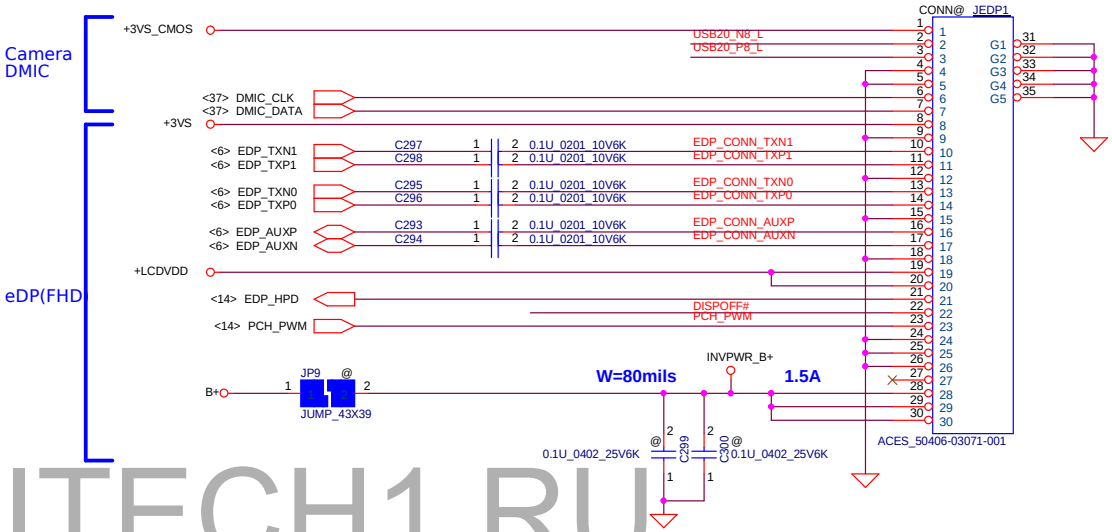
LCD POWER CIRCUIT

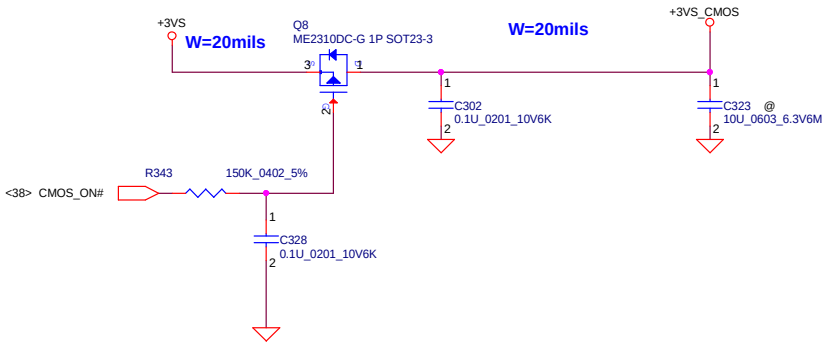


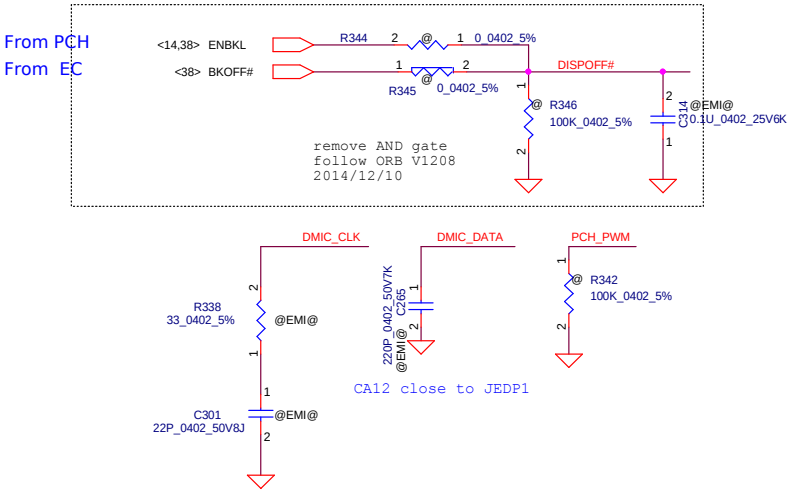


eDP(FHD) + Camera



CMOS Camera





Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **eDP LCD / Camera**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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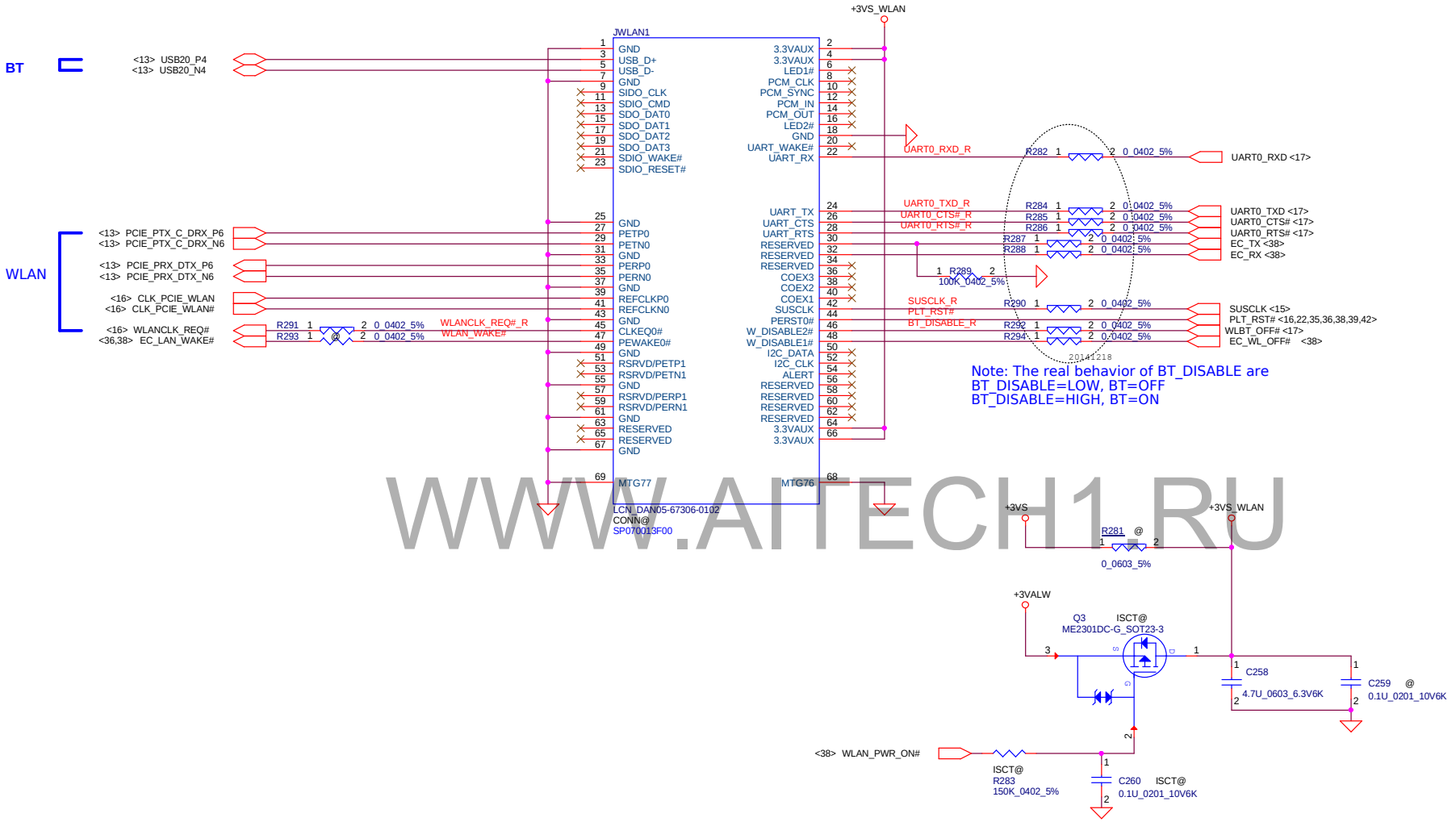
NGFF for WLAN+BT
E-KEY



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **NGFF(WLAN+BT & SSD)**

Size	Document Number	Rev
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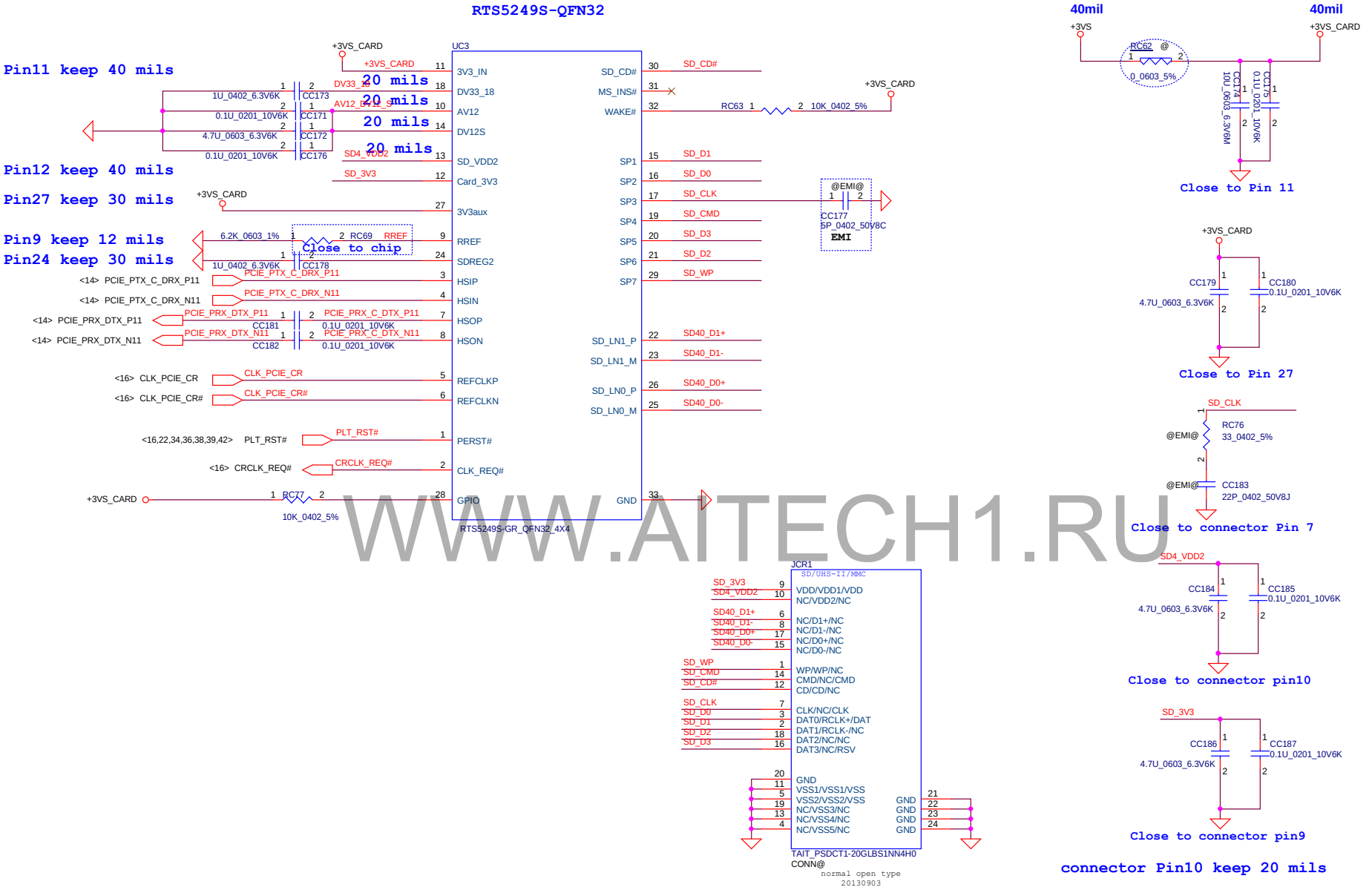
Card Reader

RTS5249S-QFN32



connector Pin10 keep 20 mils

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **CARD READER**

Size	Document Number	Rev
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+3_LAN Rising time (10 %~90 %) >1 mS and <100 mS

+3VALW — W=60mils — J2 JUMP_43X39 — 370mA — +3V_LAN

Layout Notice : Place as close chip as possible.

+3V_LAN — CL152 0.1U_0201_10V6K — These caps close to UL1 : Pin 23

LDO mode

Switching Regulator 1.0V Output from UL1 Pin24

+LAN_REGOUT — W=60mils — CL153 0.1U_0201_10V6K (Should be place within 200 mils) These components close to UL1 : Pin 24

+LAN_REGOUT — W=60mils — CL156 10U_0402_6.3V6K, CL157 0.1U_0201_10V6K, CL158 0.1U_0201_10V6K, CL159 0.1U_0201_10V6K, CL160 0.1U_0201_10V6K — close to pin 22 pin 3 pin 8 pin 30 — 1uF reserved on Pin 22

+3V_LAN — CL161 4.7U_0603_6.3V6K, CL162 0.1U_0201_10V6K, CL163 4.7U_0603_6.3V6K, CL164 0.1U_0201_10V6K — Close to UL1 : Pin 11 — Close to UL1 : Pin 32

CL165 10P 50V J NPO 0402 — XTLI — YL2 25MHZ_10PF_7V25000014 — GND GND — CL166 10P 50V J NPO 0402 — XTLO

UL1 — RTL8111H-CG_QFN32_4X4 — SA000080P00

MDI0+ MDI0- +LAN_REGOUT MDI1+ MDI1- MDI2+ MDI2- +LAN_REGOUT MDI3+ MDI3- +3V_LAN — MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N

<16> LANCLK_REQ# — <14> PCIE_RTX_C_DRX_P12 — <14> PCIE_RTX_C_DRX_N12 — <16> CLK_PCIE_LAN — <16> CLK_PCIE_LAN#

These caps close to UL1

HSOP HSON PERSTB ISOLATEB LANWAKEB DVDD10 VDDREG REGOUT LED2 LED1/GPIO LED0 CKXTAL1 CKXTAL2 AVDD10 RSET AVDD33 GND

PCIE_PRX_C_DTX_P12 — CL167 0.1U_0201_10V6K — PCIE_PRX_DTX_P12 — PCIE_PRX_DTX_P12 <14>

PCIE_PRX_C_DTX_N12 — CL168 0.1U_0201_10V6K — PCIE_PRX_DTX_N12 — PCIE_PRX_DTX_N12 <14>

ISOLATEB — ISOLATEB

+LAN_REGOUT — +3V_LAN — +LAN_REGOUT — PLT_RST# <16,22,34,35,38,39,42>

+LAN_REGOUT — EC_LAN_WAKE# <34,38>

TPL190 — TPL191 — XTLO — XTLI — +LAN_REGOUT — LAN_RSET — +3V_LAN

LED1_GPIO — RL1 10K_0402_5% — +3V_LAN — reserved GPIO pin

RL60 2.49K_0402_1%

+3VS — RL58 1K_0402_5% — ISOLATEB — RL59 15K_0402_5%

TL1 — NS892407 1G — SP050006800

TCT — MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3- — TCT1 TD1+ TD1- TCT2 TD2 TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4- — MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4- — MCT — MDO0+ MDO0- MDO1+ MDO1- MDO2+ MDO2- MDO3+ MDO3-

CL170 0.01U_0402_50V7K EMI@ — CL171 @EMI@ 5P_0402_50V8C — Reserve for EMI

RL61 EMI@ 75_0805_5% — EMI@ CL169 10P_0603_50V8-J — DL1 BS4200N-C-LV_SMB-F2 EMI@ SCV00001D00 — CHASSIS1_GND

EMI@ DL3 — MDI3+ MDI3- MDI2+ MDI2- — I/O1 I/O2 GND I/O3 VDD I/O4 — AZC099-04S.R7G_SOT23-6 SC300001G00

EMI@ DL2 — MDI1+ MDI1- MDI0+ MDI0- — AZC099-04S.R7G_SOT23-6 SC300001G00

@EMI@ RL2 0_0402_5% — CHASSIS1_GND

@EMI@ RL3 0_0402_5% — CHASSIS2_GND

JRJ1 CONN@ — SINGA_2RJ3081-018211F — DC23400AS00

MDO0+ MDO0- MDO1+ MDO2+ MDO2- MDO1- MDO3+ MDO3- — PR1+ PR1- PR2+ PR3+ PR3- PR2- PR4+ PR4-

GND GND GND GND — CHASSIS1_GND — CHASSIS2_GND

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: LAN_RTL8111H-CG

Size: Custom | Document Number: LA-C951P | Rev: 1.0

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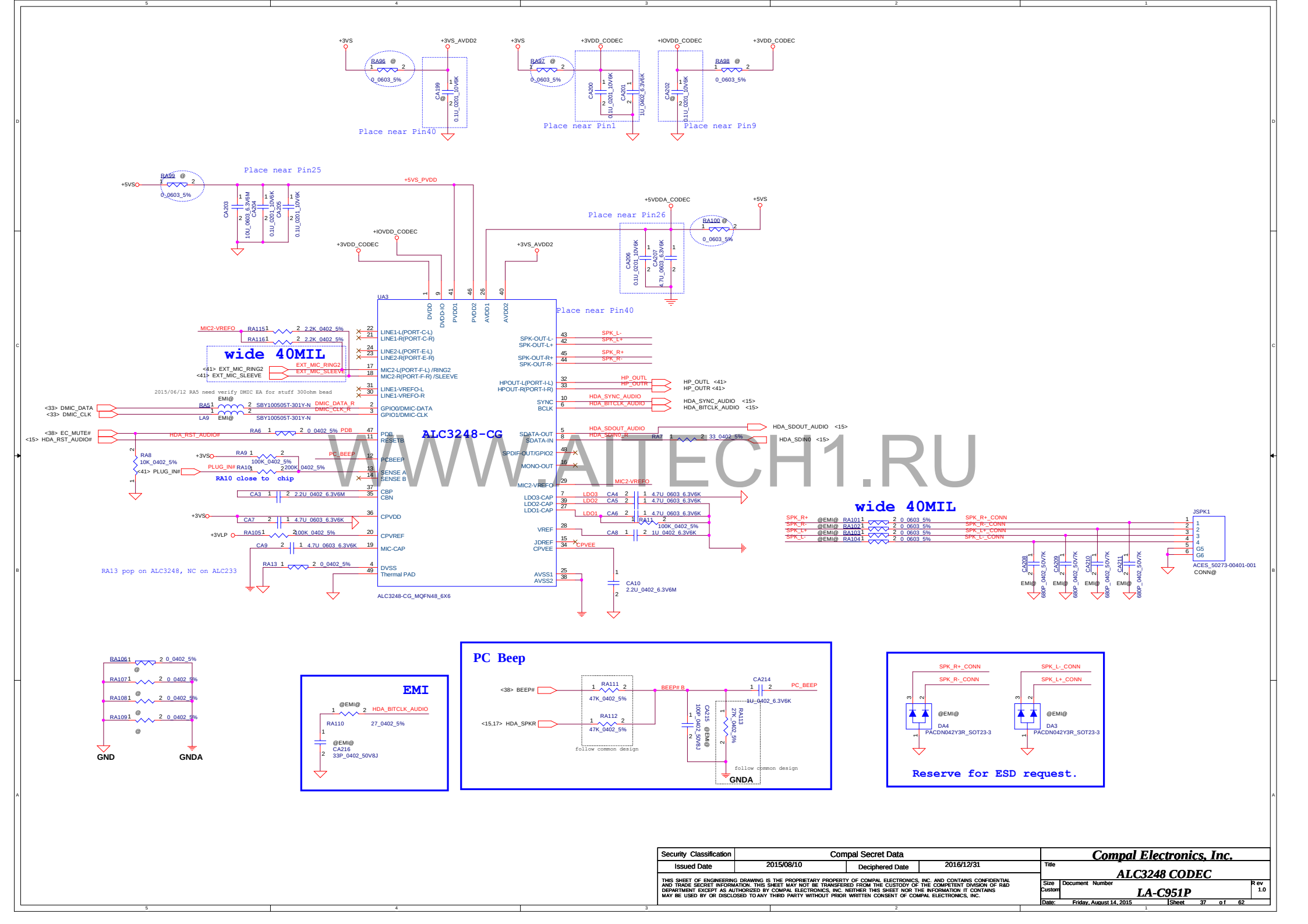

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **ALC3248 CODEC**

Size	Document Number	Rev
Custom	LA-C951P	1.0

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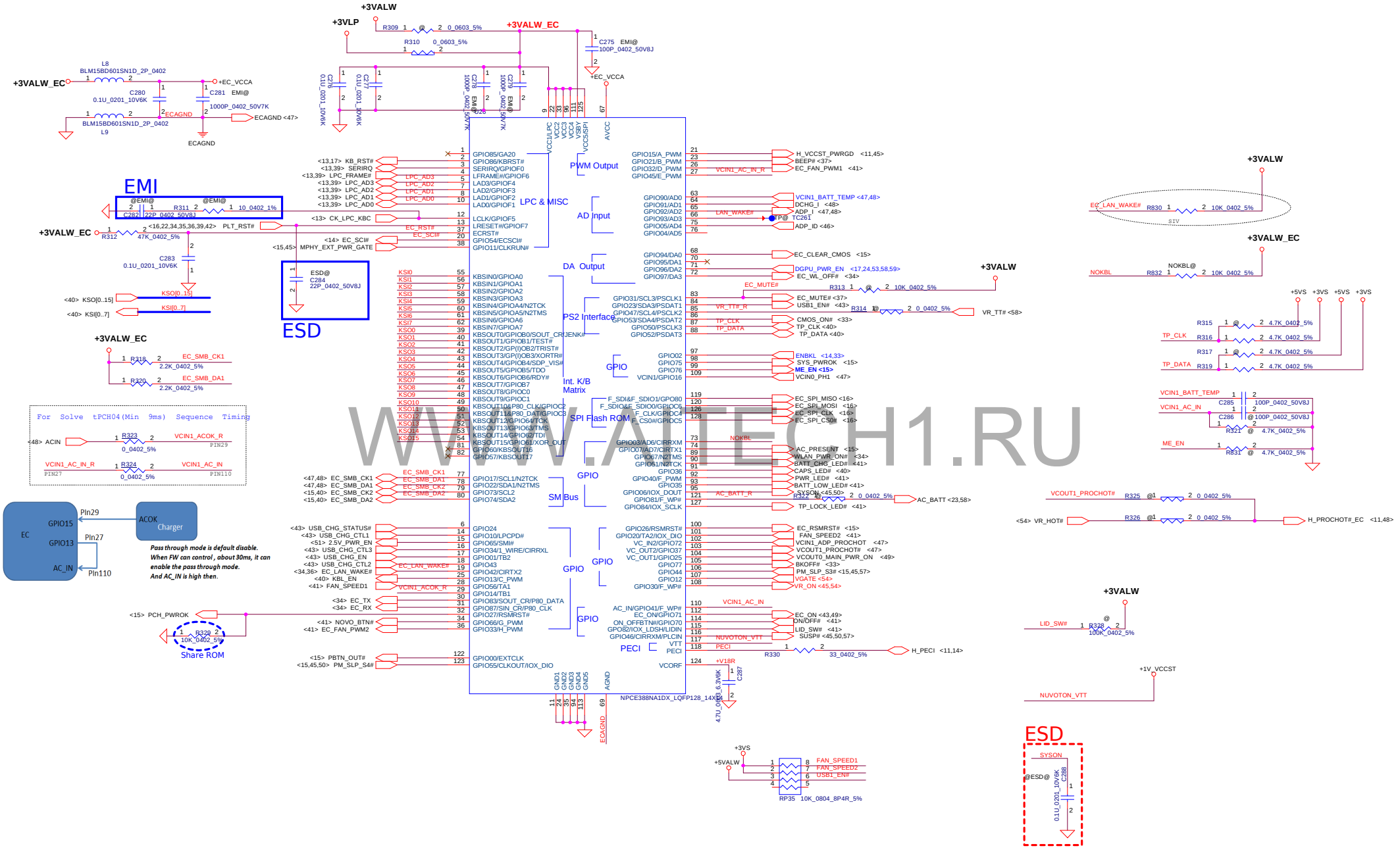

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
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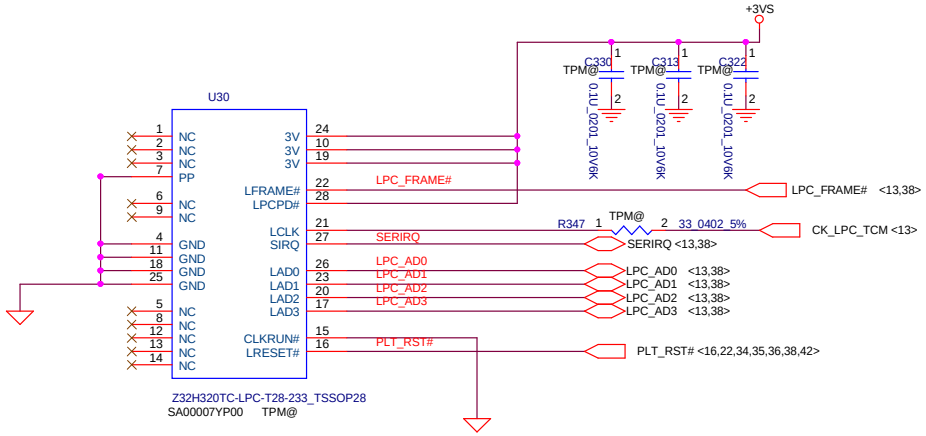

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **TPM**

Size	Document Number	Rev
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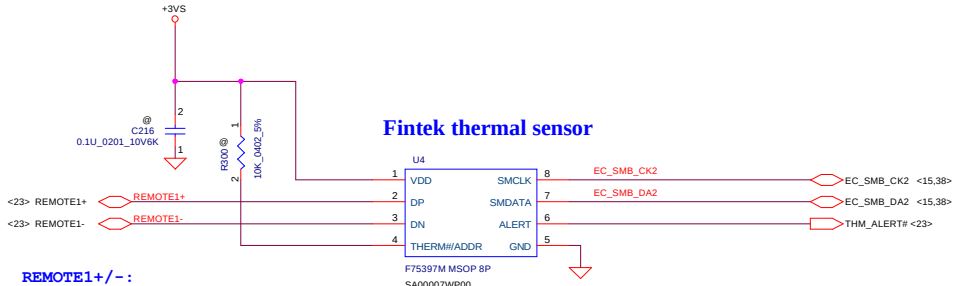
Thermal Sensor

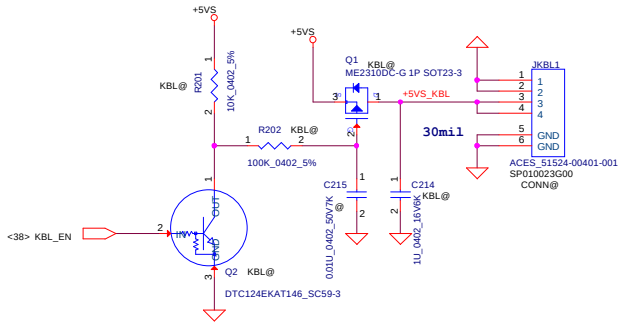


Fintek thermal sensor

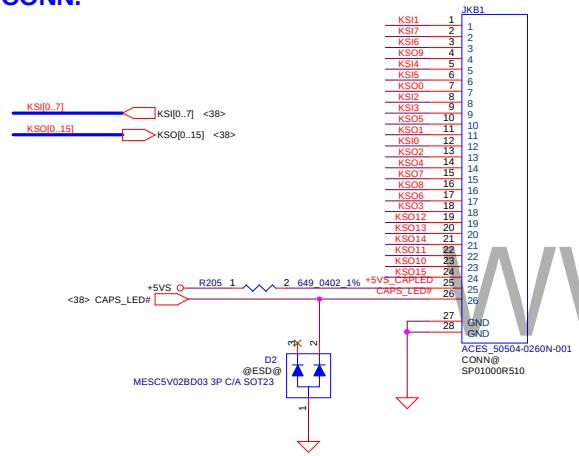
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

Address 100_1100b

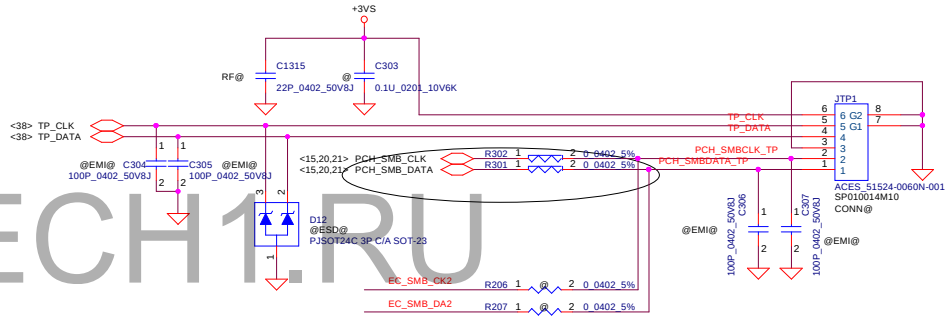
KB BKL



KB CONN.



TP CONN.



Screw

CPU

H14 HOLEA H_3P7
H2 HOLEA H_3P7
H3 HOLEA H_3P7

H4 HOLEA CHASSIS2_GND H_3P3
H18 HOLEA CHASSIS1_GND H_3P3
H10 HOLEA CHASSIS1_GND H_2P5

Board side

H6 HOLEA H_2P5
H7 HOLEA H_2P5
H8 HOLEA H_2P5
H9 HOLEA H_4P1X3P1N
H11 HOLEA H_3P0-G
H12 HOLEA H_2P5
H21 HOLEA H_4P1
H22 HOLEA H_2P5-G
H23 HOLEA H_2P5-G
H24 HOLEA H_4P4X3P4N
H25 HOLEA H_2P0N

CLIP1 HOLEA
CLIP2 HOLEA
CLIP3 HOLEA
CLIP4 HOLEA
CLIP5 HOLEA
CLIP6 HOLEA

GPU

H13 HOLEA H_3P7
H1 HOLEA H_3P7
H15 HOLEA H_3P7

LAN

H16 HOLEA H_1P5N
H17 HOLEA H_1P5N

NGFF

H5 HOLEA H_3P3

FD1
FD2
FD3
FD4

Zero point

H19 HOLEA H_3P1N

Fan

H20 HOLEA H_1P3X1P8N

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **KB/TP/Thermal Sensor**

Size	Document Number	Rev
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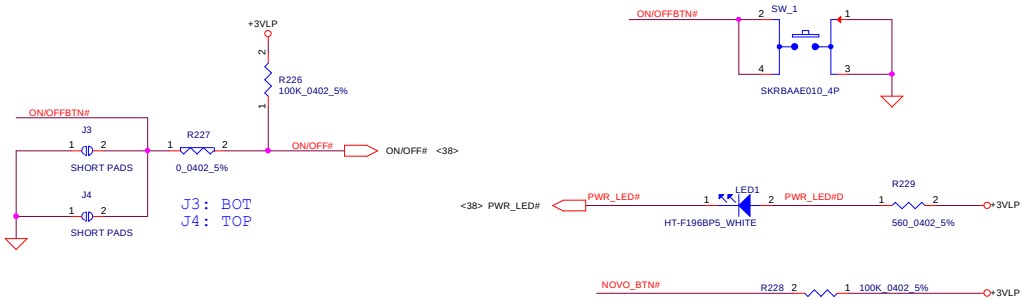
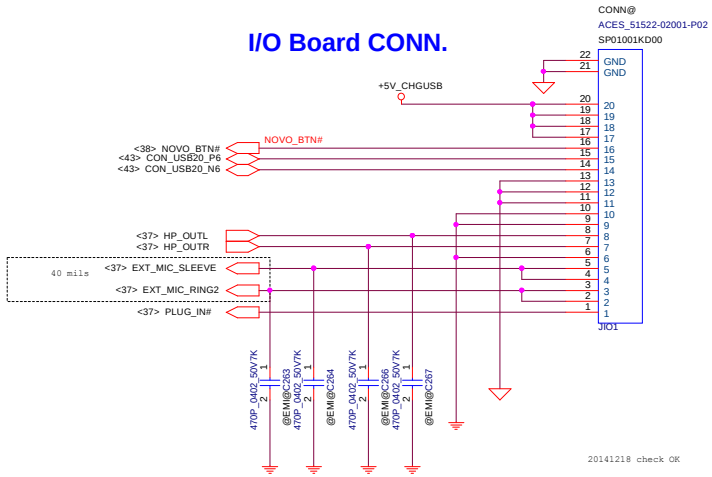
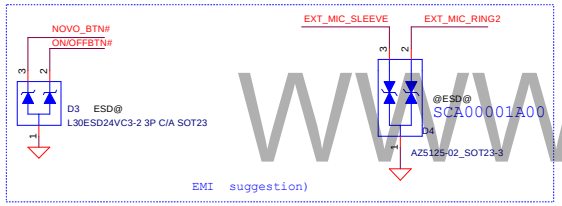
Power BTN.

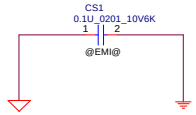
Power_BTN



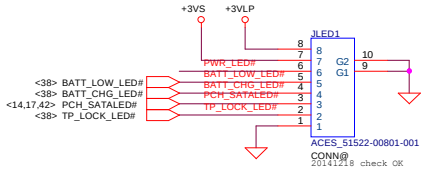
I/O Board CONN.

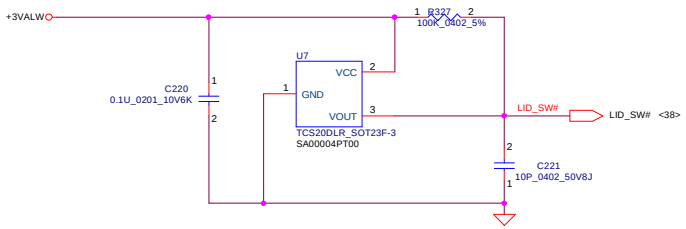




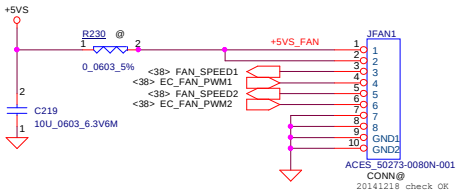


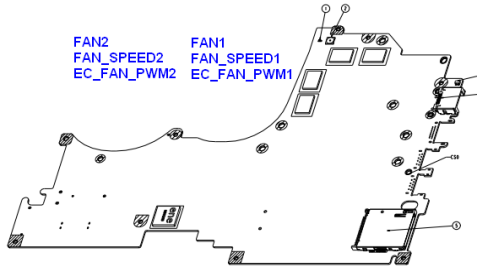
LED Board CONN.





FAN1 Conn



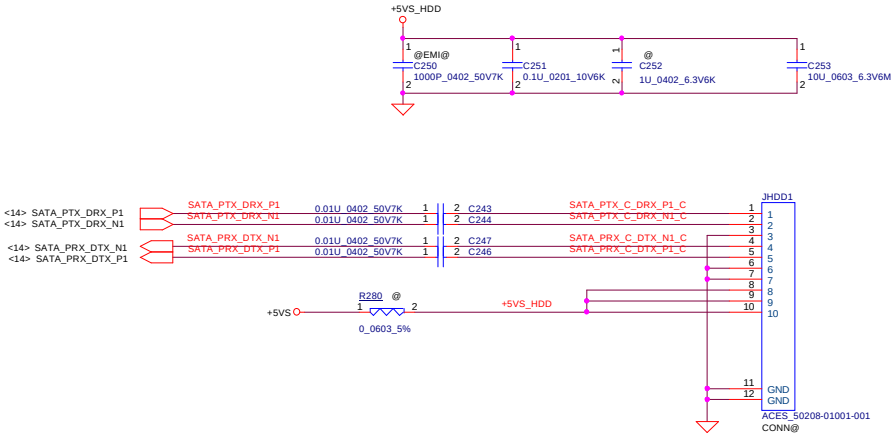


FAN2	FAN1
FAN_SPEED2 EC_FAN_PWM2	FAN_SPEED1 EC_FAN_PWM1

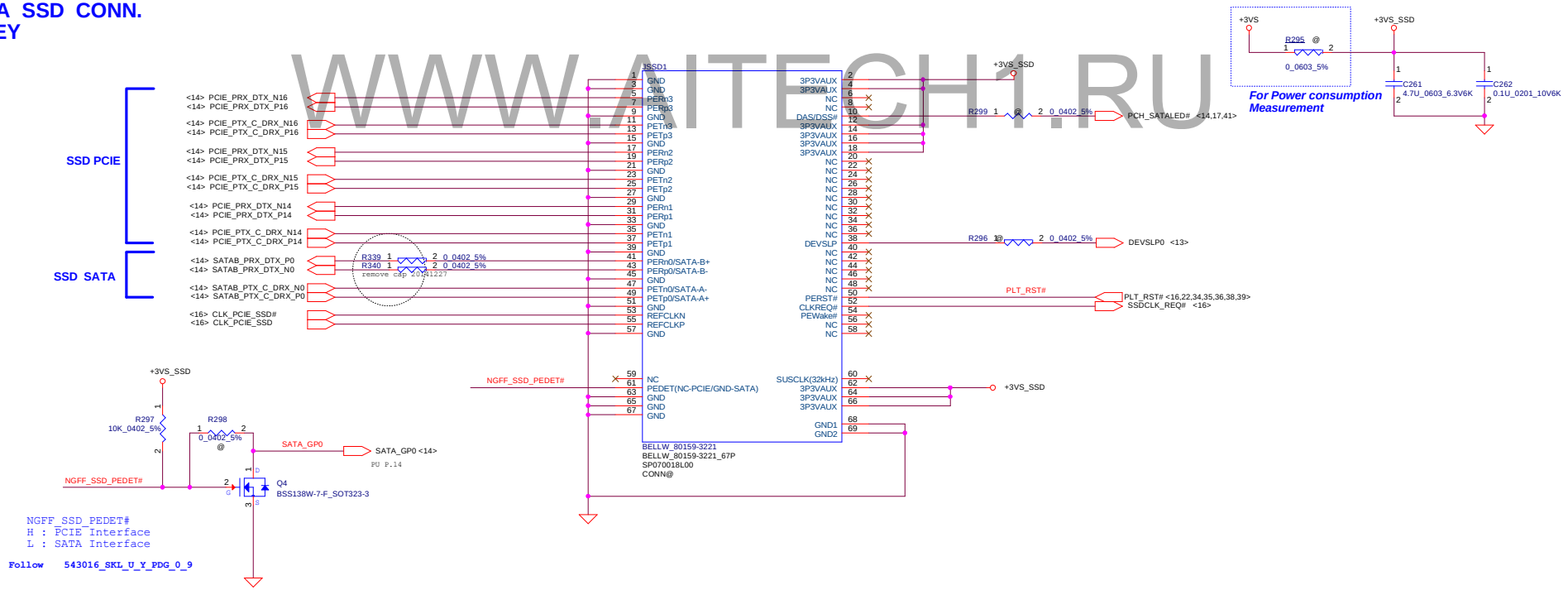
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title: FAN/PWR/LED/IO Board			
Size: Custom	Document Number: LA-C951P		Rev: 1.0
Date: Friday, August 14, 2015	Sheet 41 of 62		

SATA HDD Conn.



SATA SSD CONN. M-KEY



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

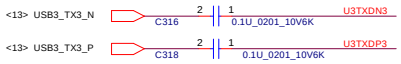
Compal Electronics, Inc.

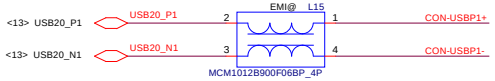
Title: **HDD REPETER**

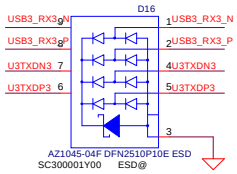
Size	Document Number	Rev
Custom	LA-C951P	1.0

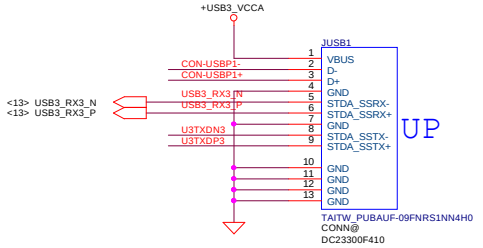
Date: Friday, August 14, 2015 Sheet 42 of 62

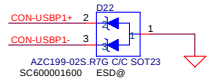
USB3.0 <Port1,Port2>

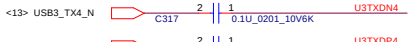


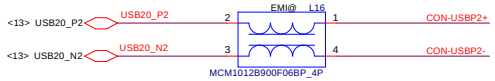


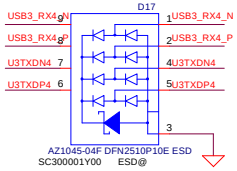


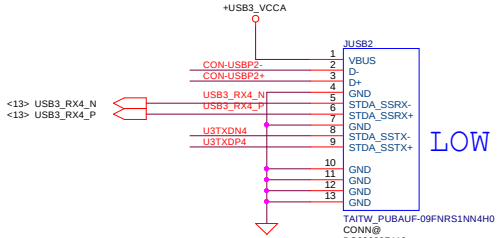


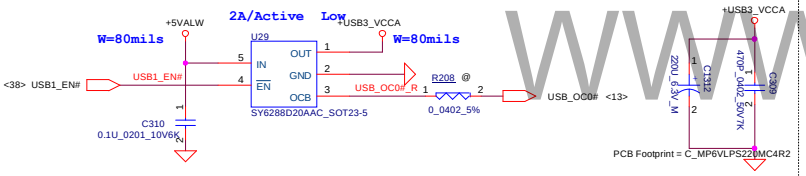




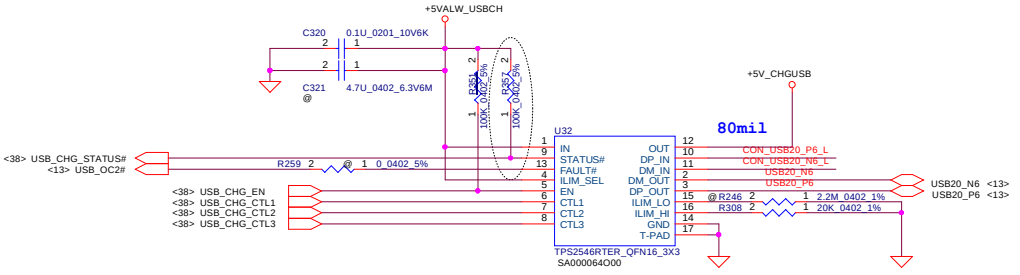


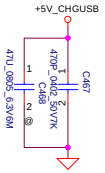


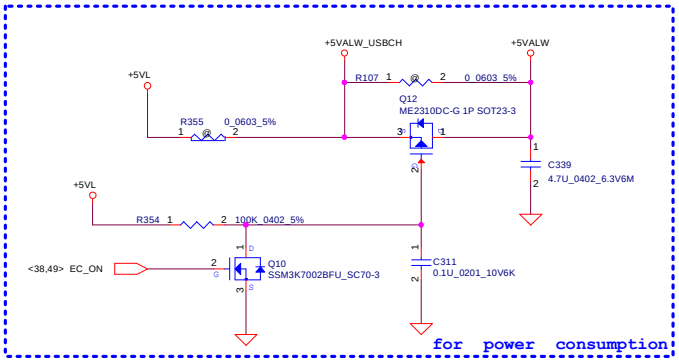




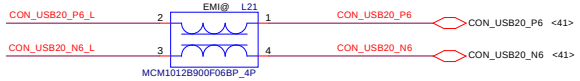
USB2.0 + Charger







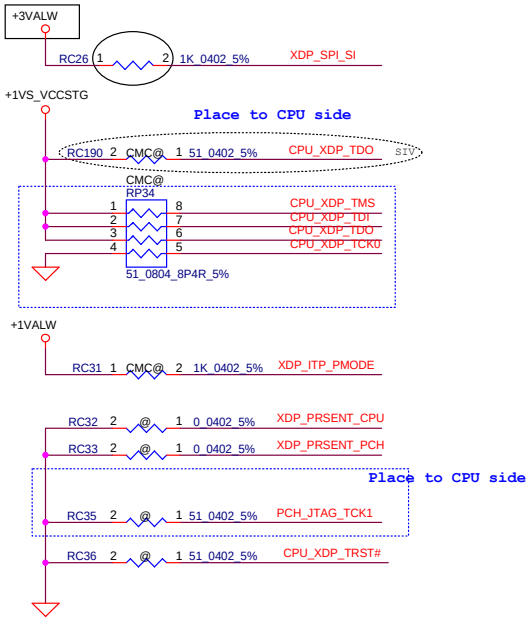
	CTL1	CTL2	CTL3
S0	H	H	H
S3	H	H	H
DC S5	L	L	H

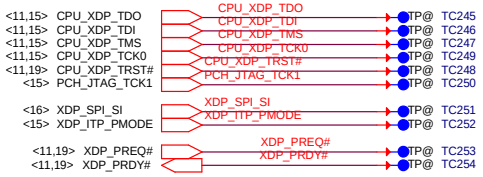


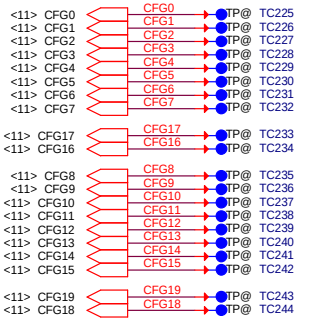
Security Classification	Compal Secret Data	
Issued Date	2015/08/10	Deciphered Date 2016/12/31

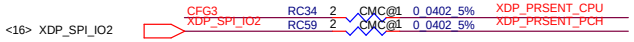
Compal Electronics, Inc.	
Title	USB2.0/3.0
Size: Custom	Document Number: LA-C951P
Rev	1.0
Date: Friday, August 14, 2015	Sheet 43 of 62

PRIMARY CMC TP









Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

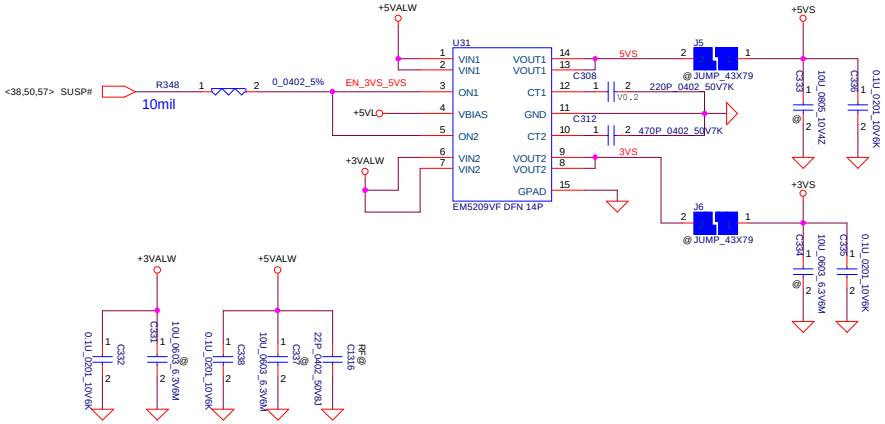
Compal Electronics, Inc.

Title: **CMC debug port**

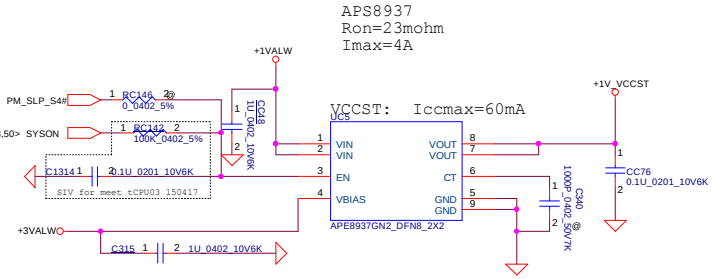
Size	Document Number	Rev
Custom	LA-C951P	1.0

Date: Friday, August 14, 2015 | Sheet 44 of 62

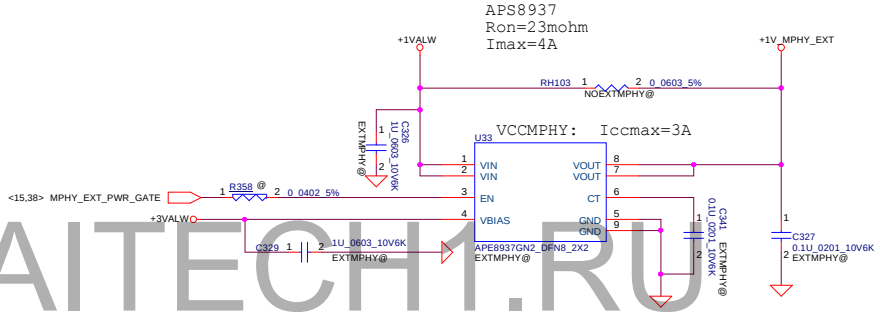
+5VALW TO +5VS
+3VALW TO +3VS



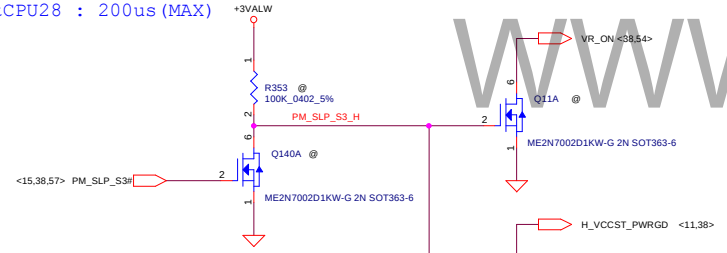
+1VALW TO +VCCST



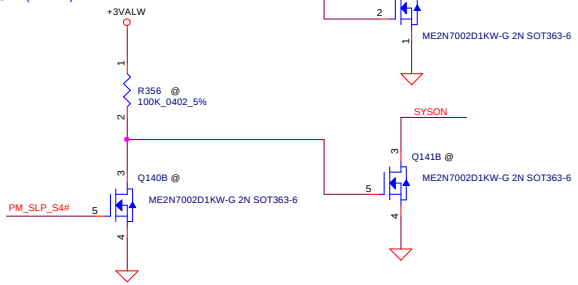
+1VALW TO +VCCMPHY



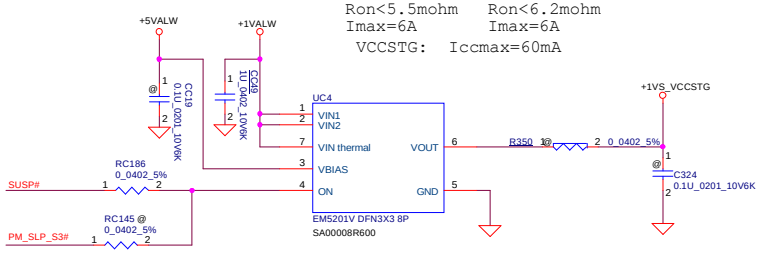
For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 200us (MAX)
tPLT18 : 200us (MAX)
tCPU28 : 200us (MAX)



For meet tPLT15 power down sequence.
tPLT15 : 200us (MAX)



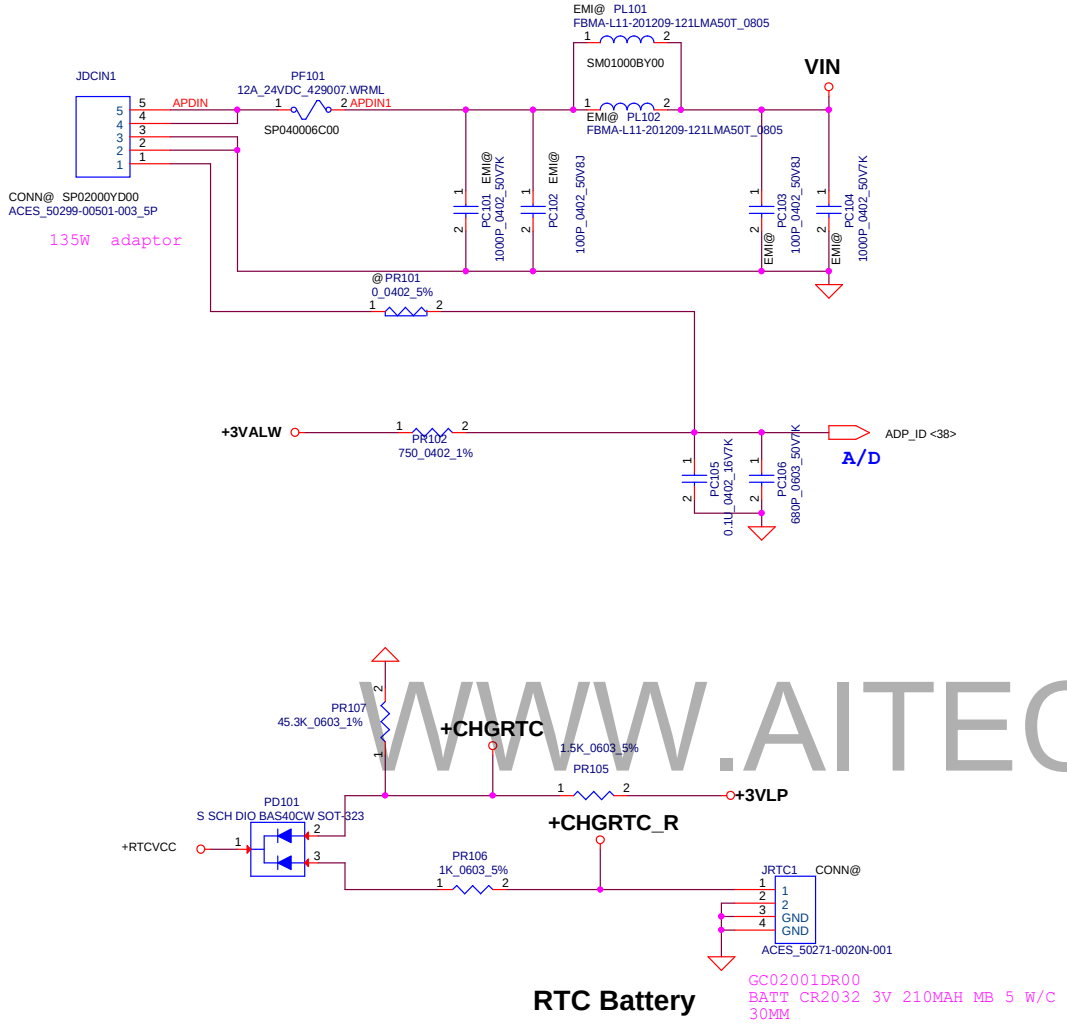
+1VALW TO +VCCSTG



V1.00A	SLP_SUS#	1.00 V	5.885	NA	NA	V1.00A	3.46
				<= 65usec full load ready	SLP_S3# AND SLP_S0#	Vcc_{STG}	0.06
				NA	NA	Vcc_{MPHYG}	2.10
				<= 65usec full load ready (Note 11)	SLP_S4#	Vcc_{ST}	0.12
						Vcc_{PLL}	0.145

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.	
Title	DC/DC Interface
Size / Document Number	LA-C951P
Custom	Rev 1.0
Date: Friday, August 14, 2015	Sheet 45 of 62



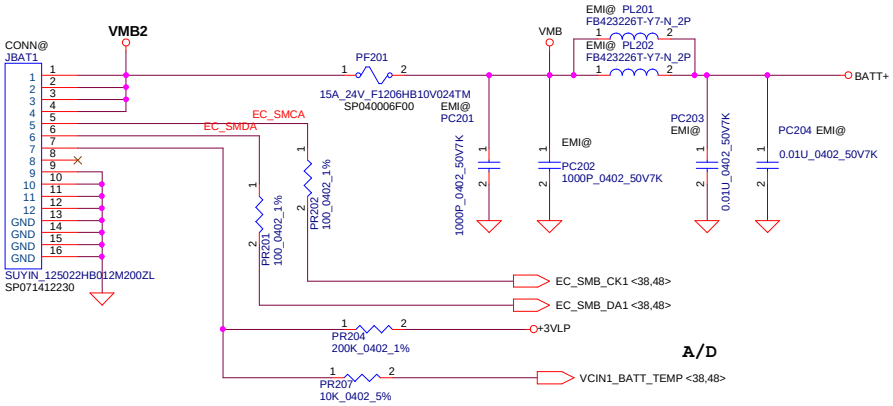
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

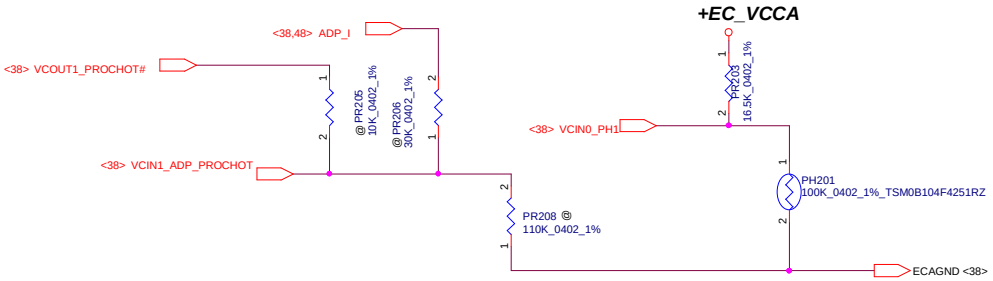
Compal Electronics, Inc.

Title: ***PWR DCIN / RTC battery***

Size	Document Number	Rev
	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 46 of 62





ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

B+ near 5V input

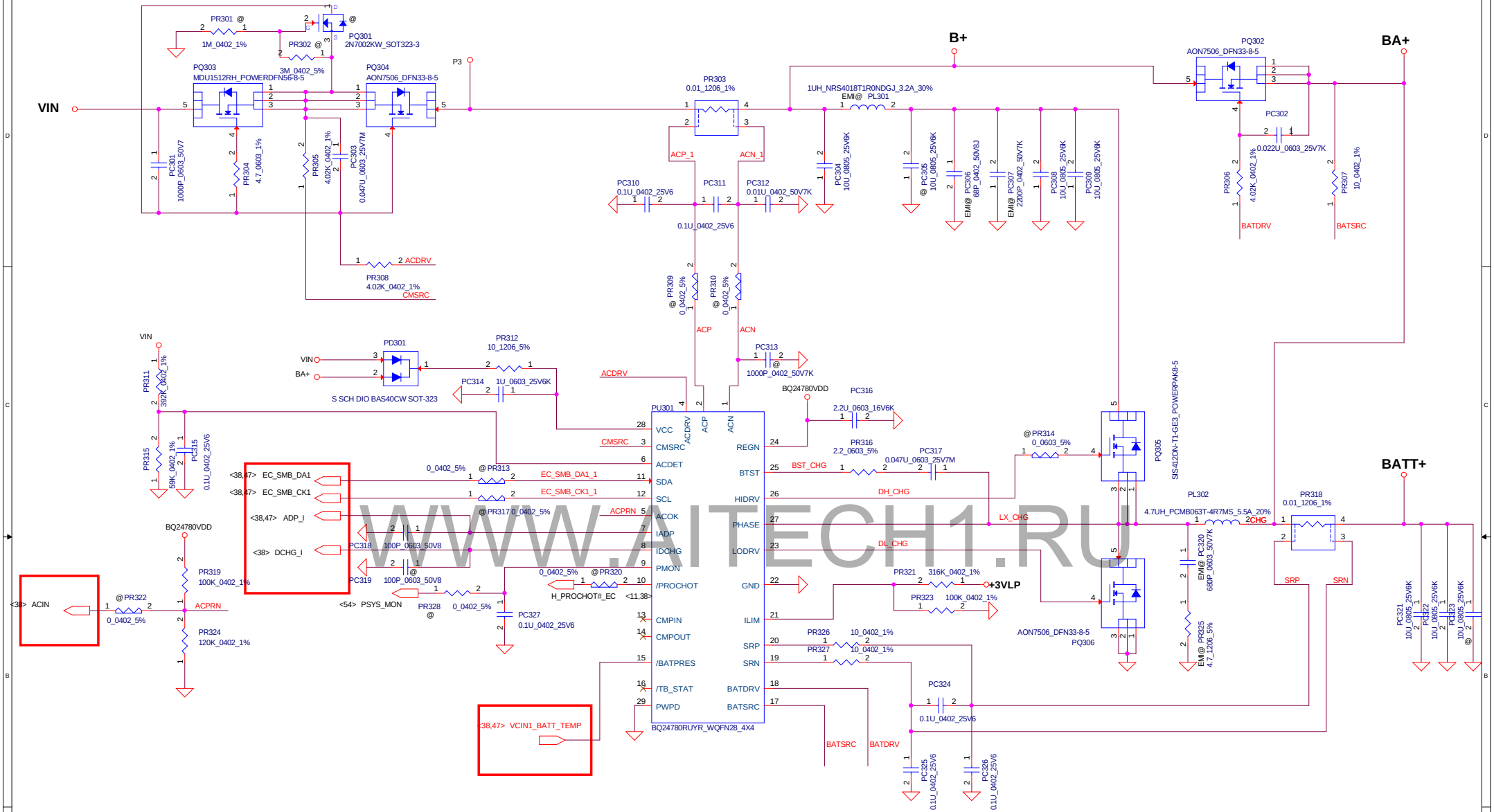
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 47 of 62



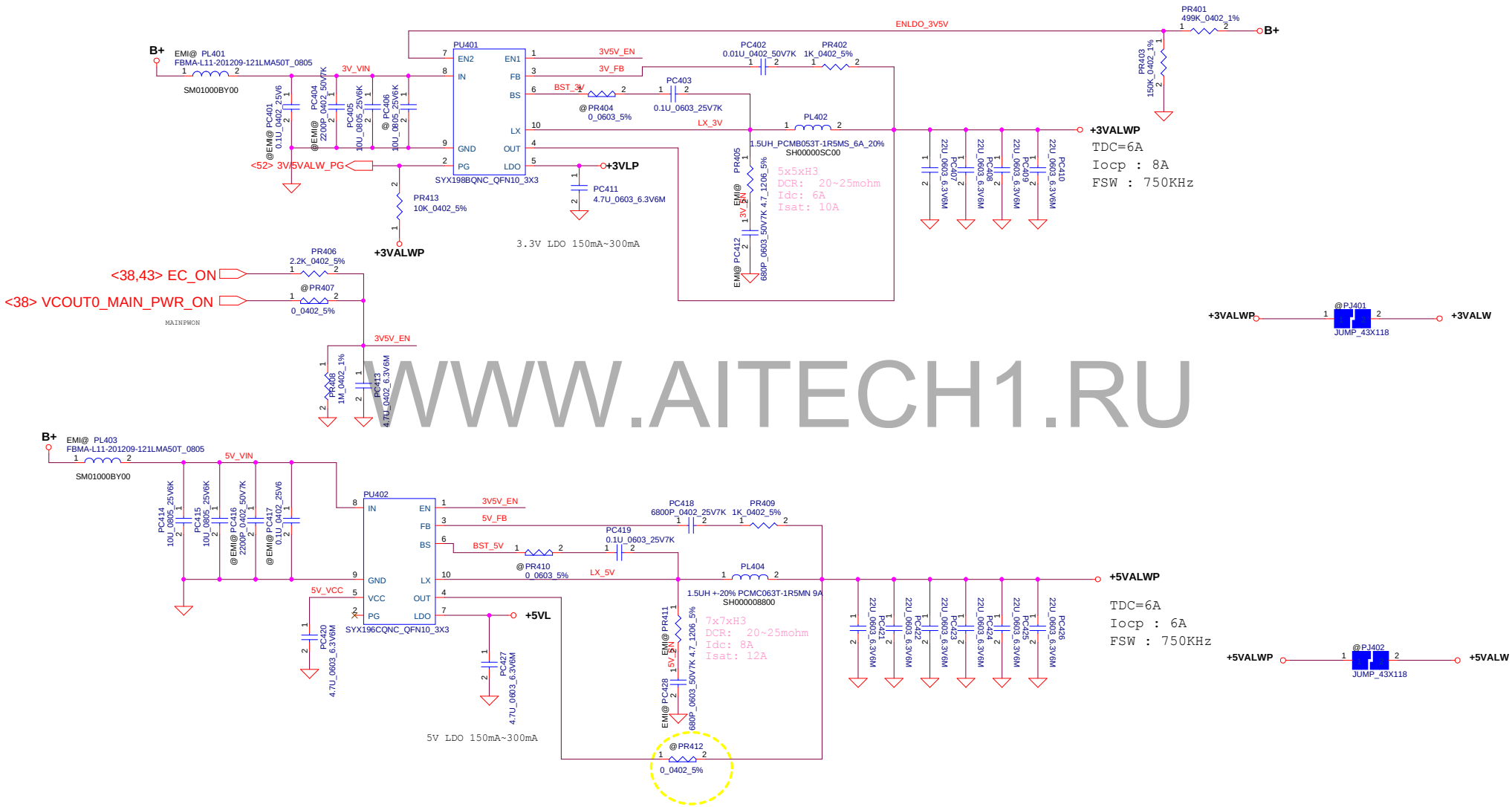
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **Charger BQ24780**

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 48 of 62



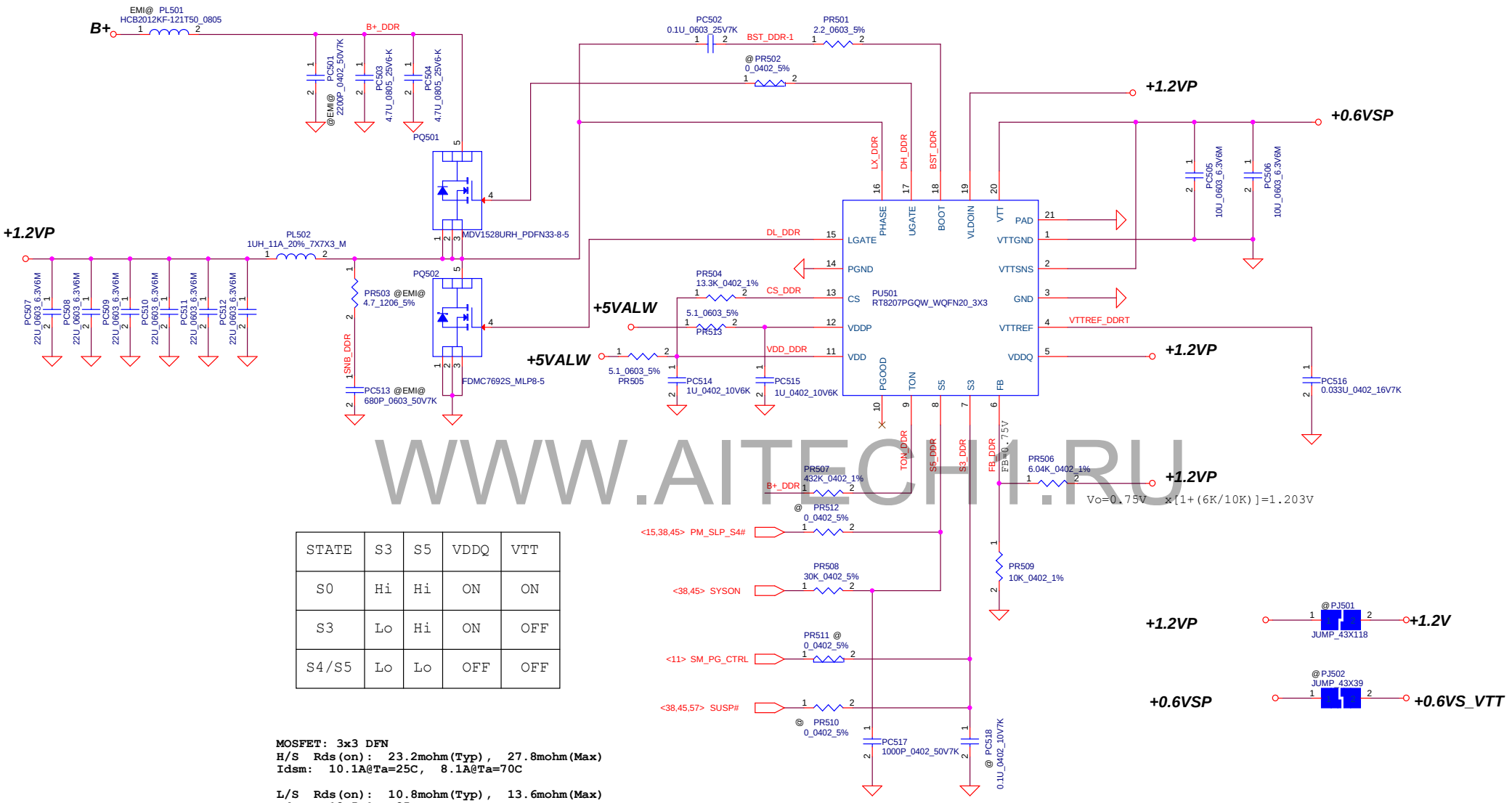
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 49 of 62



STATE	S3	S5	VDDQ	VTT
S0	Hi	Hi	ON	ON
S3	Lo	Hi	ON	OFF
S4/S5	Lo	Lo	OFF	OFF

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 10.8mohm(Typ), 13.6mohm(Max)
Idsm: 12.5A@Ta=25C

Choke: 7x7x3
Rdc=6.2mohm(Typ), 11mohm(Max)

Switching Frequency: 285kHz
Ipeak=9.3A
Iocp~12.3A
OVP: 113%~120%
VFB=0.75V, Vout=1.2V
MOSFET footprint: SIS412DN

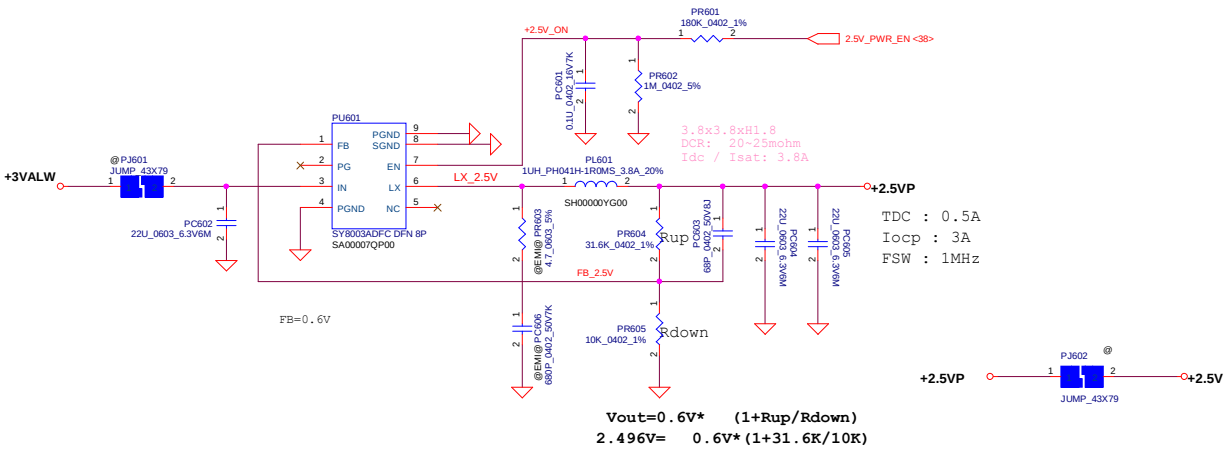
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: DDR RT8207P

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 Sheet 50 of 62



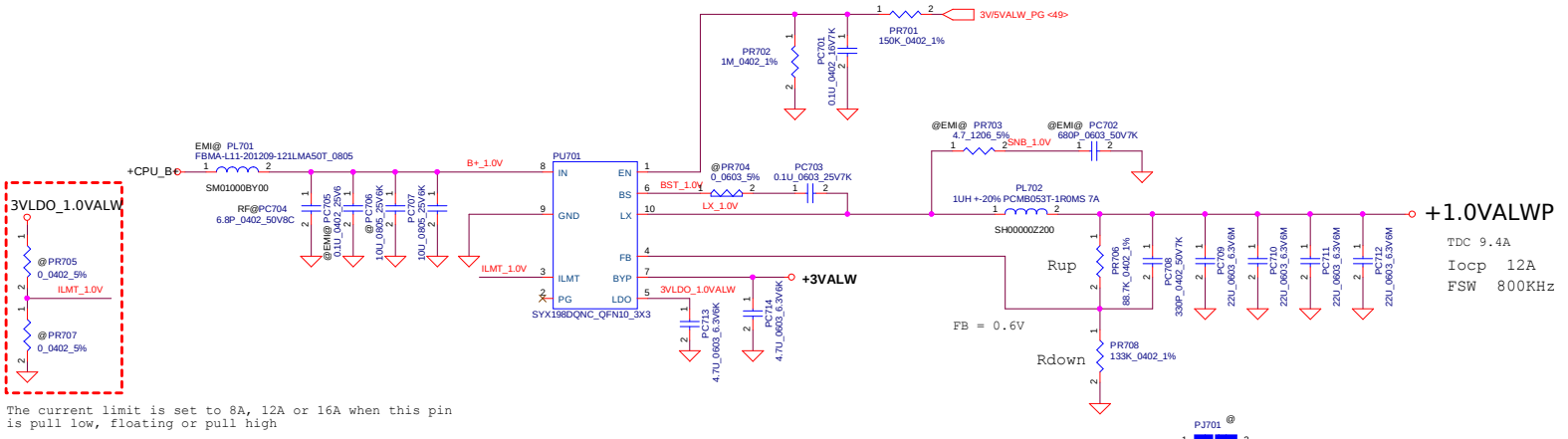
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: 2.5V

Size: Custom | Document Number: SKL_H 42 | Rev: 1.0

Date: Friday, August 14, 2015 | Sheet 51 of 62



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
1.0V=0.6V* (1+88.7K/133K)

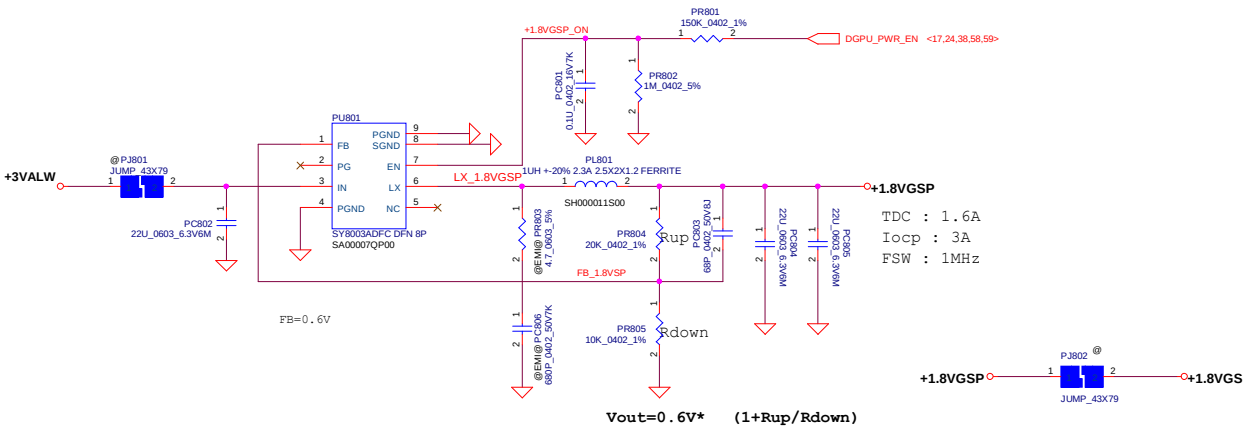
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: 1.0V

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 Sheet 52 of 62



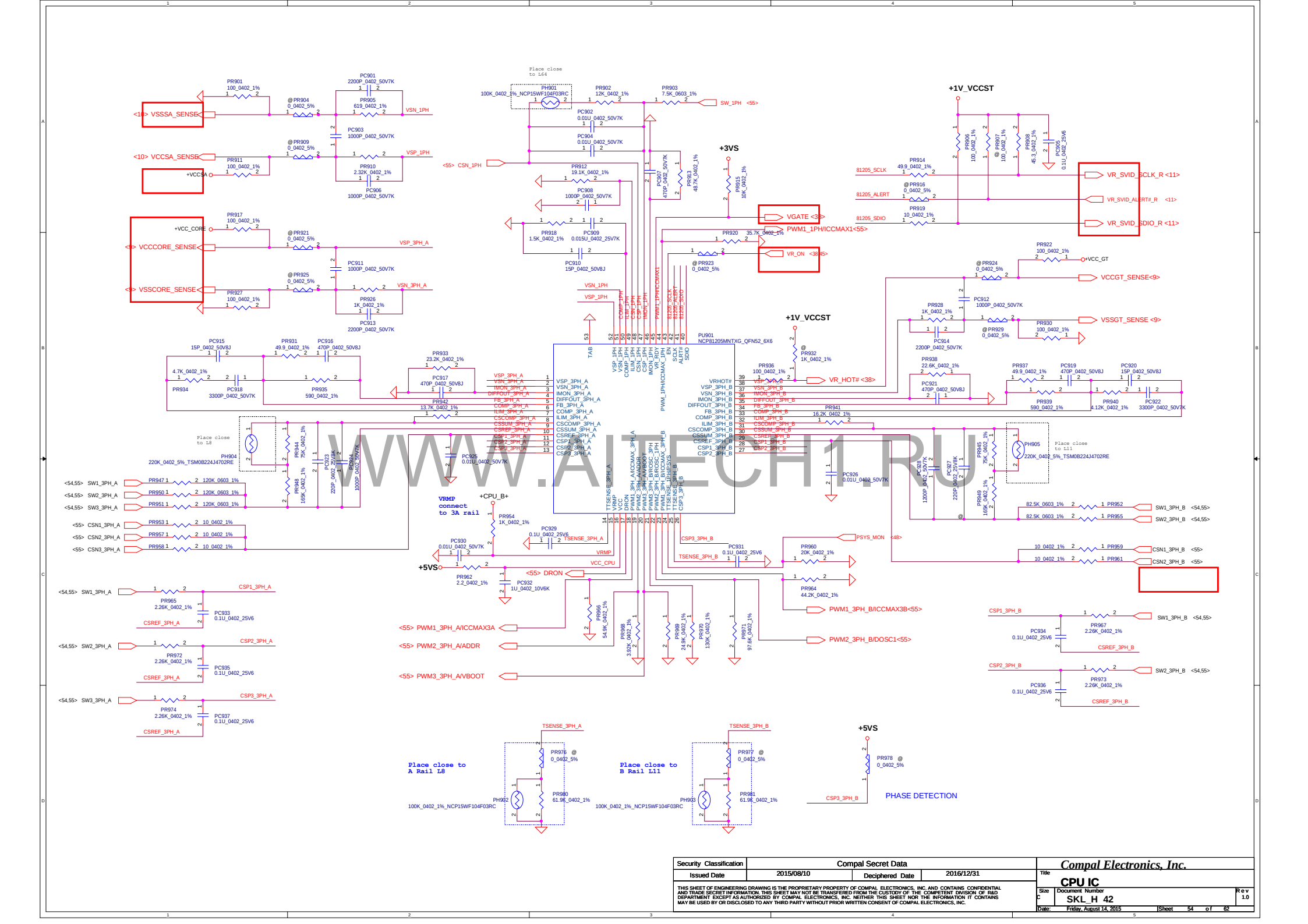
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **1.8V / 1.5V**

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 53 of 62



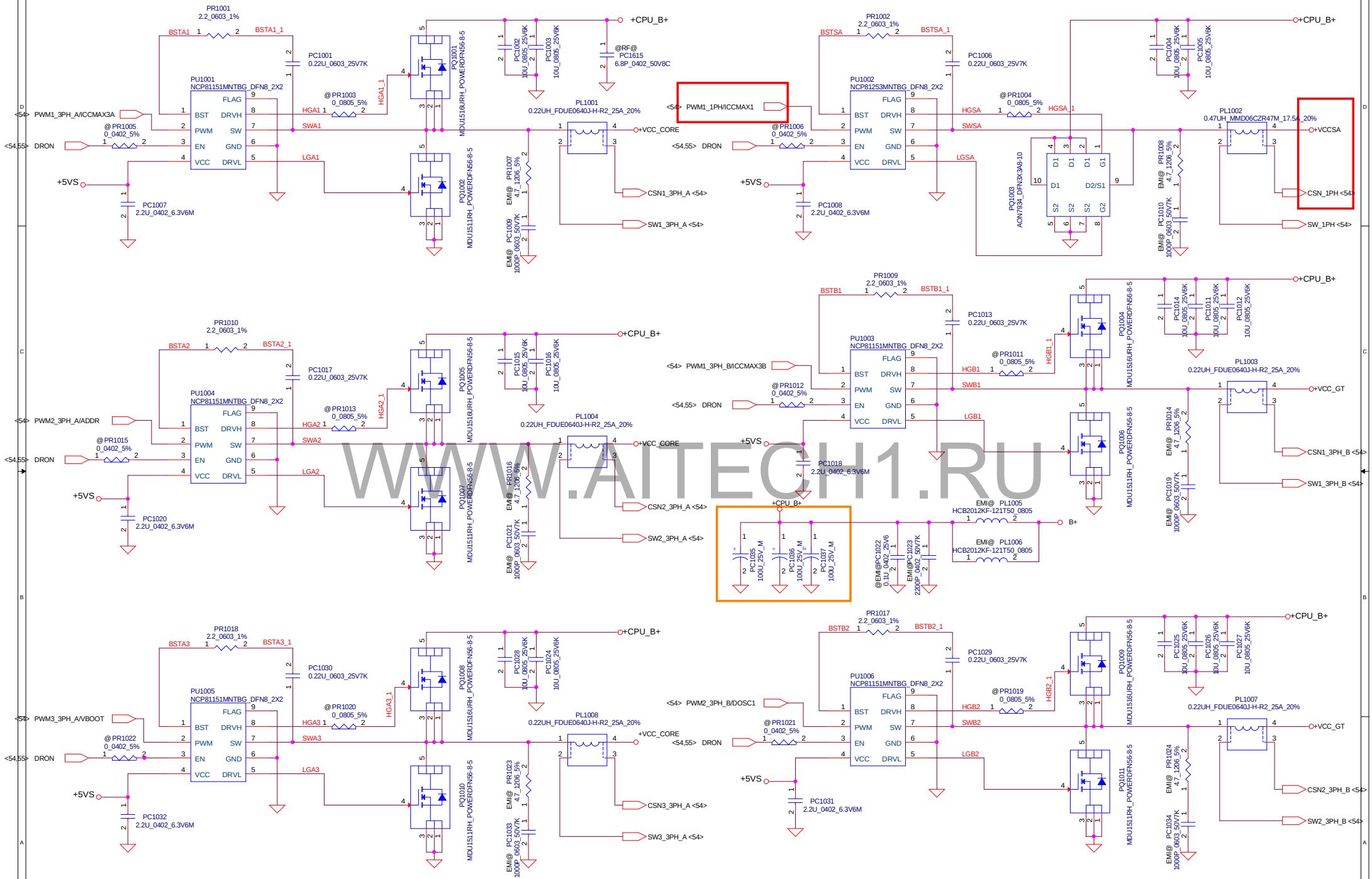
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: CPU IC

Size	Document Number	Rev
C	SKL_H 42	1.0

Date: Friday, August 14, 2015 Sheet 54 of 62



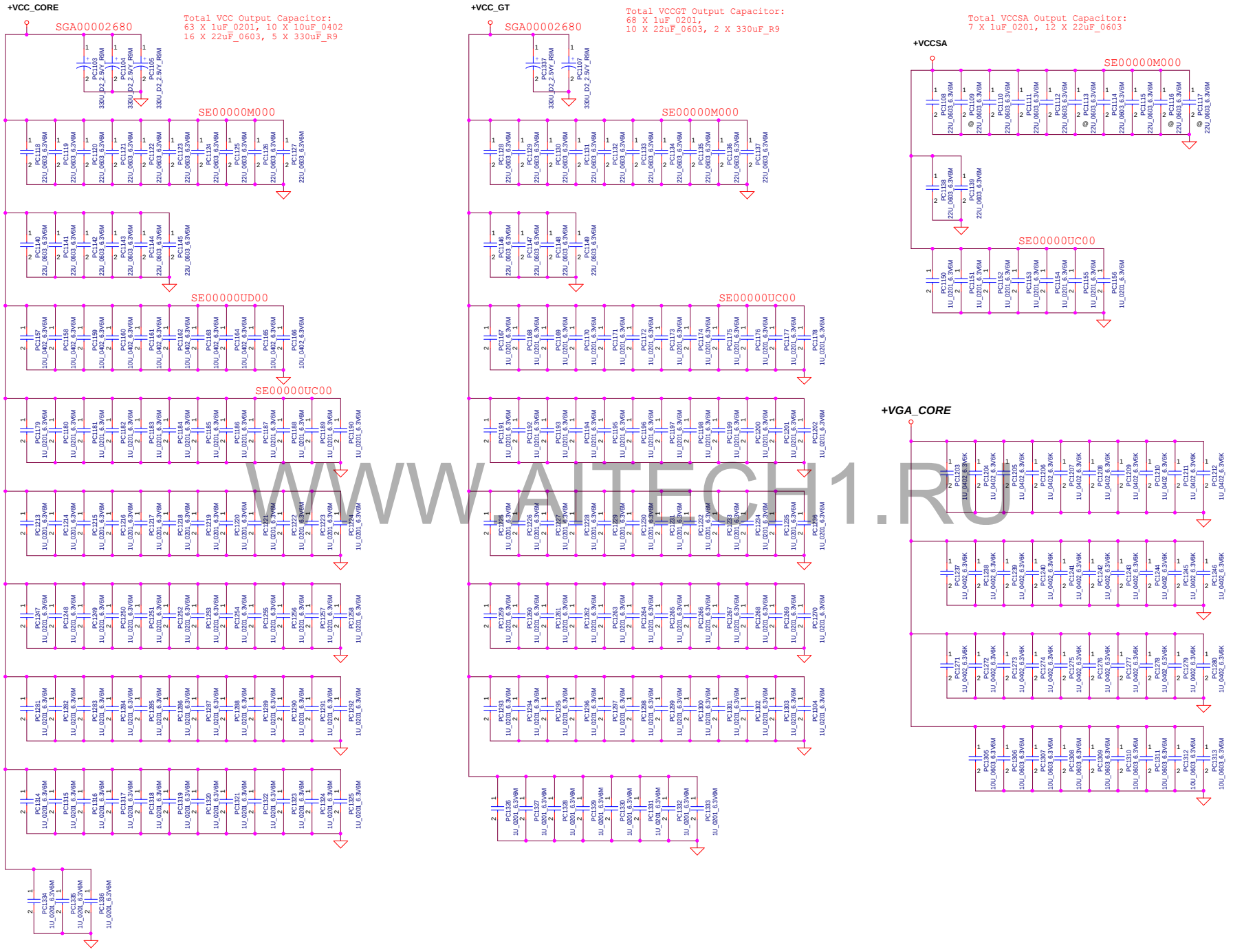
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 55 of 62



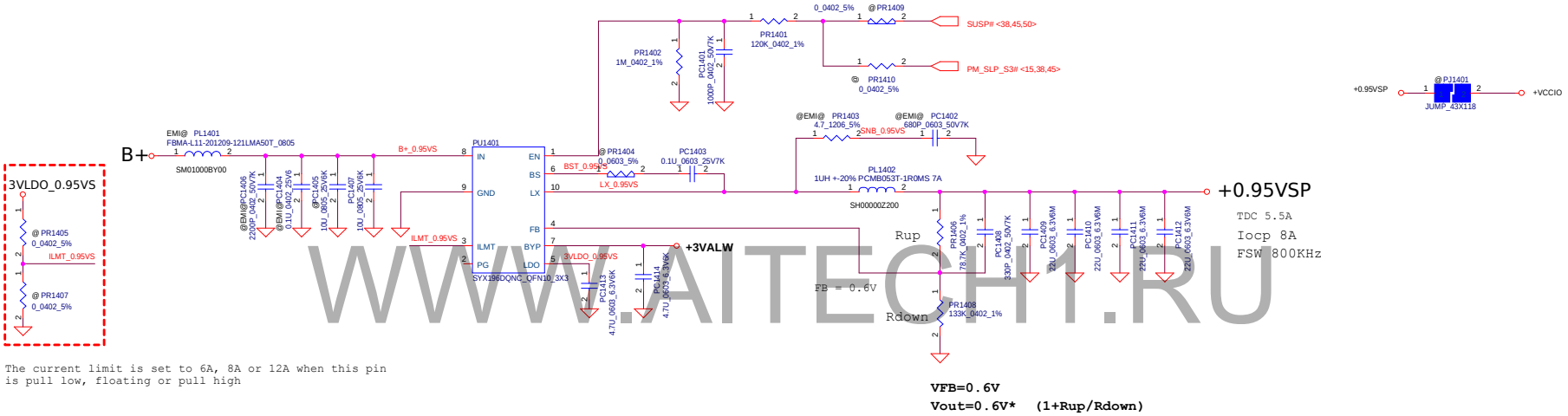
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: Processor decoupling

Size	Document Number	Rev
C	SKL_H 42	1.0

Date: Friday, August 14, 2015 Sheet 56 of 62



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

VFB=0.6V

Vout=0.6V* (1+Rup/Rdown)

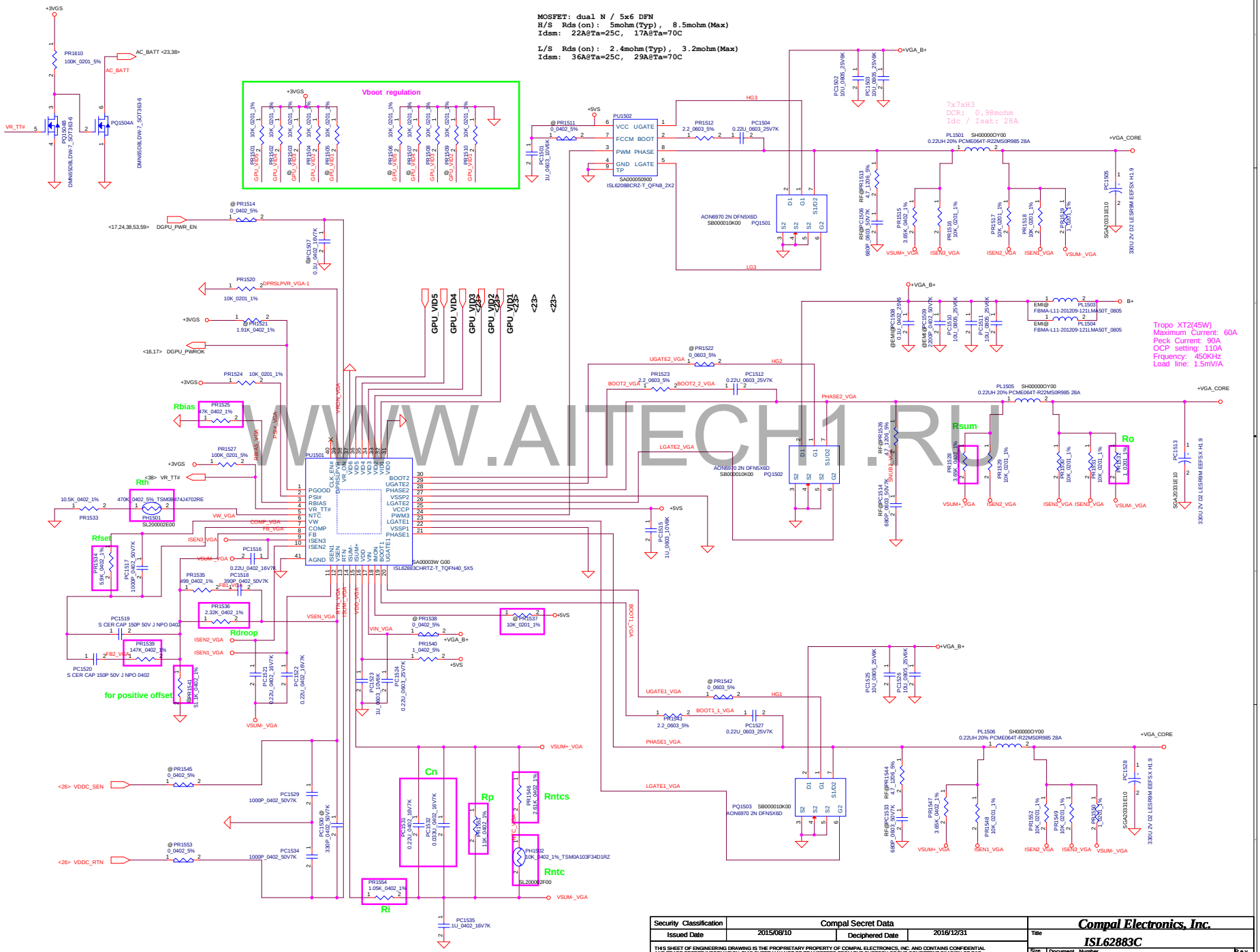
Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **0.95VS**

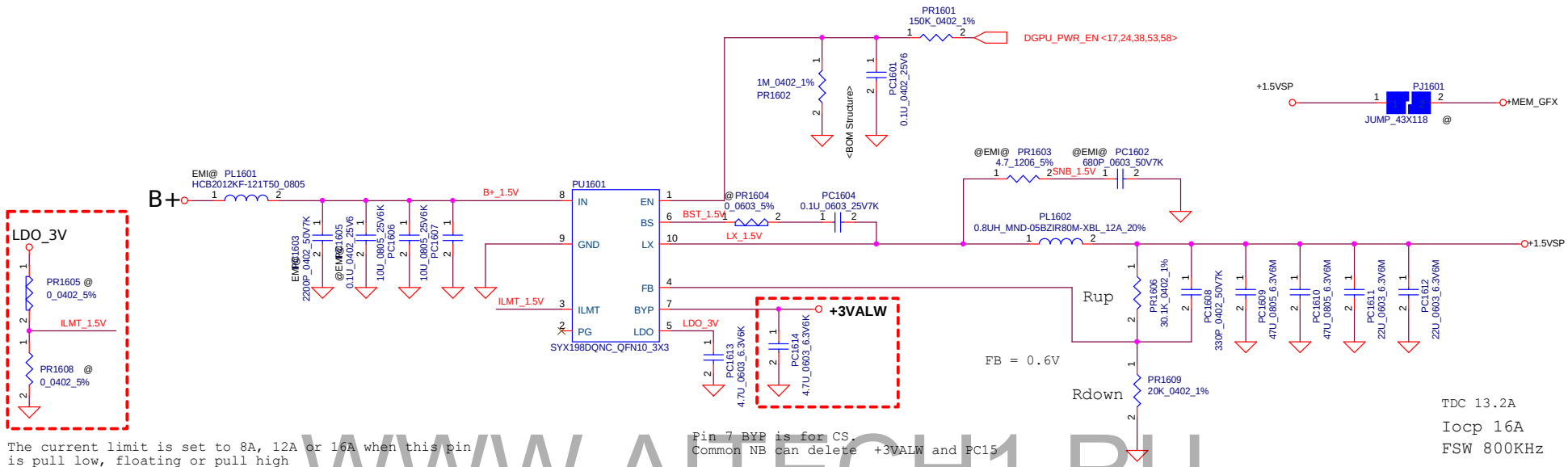
Size	Document Number	Rev
C	SKL_H 42	1.0

Date: Friday, August 14, 2015 Sheet 57 of 62



Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.			
Title	ISL62883C		
Size	Document Number		Rev
	SKL_H 42		1.0
Date: Friday, August 14, 2015	Sheet 58 of 62		



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

TDC 13.2A
Iocp 16A
FSW 800KHz

VFB=0.6V

Vout=0.6V* (1+Rup/Rdown)

Vout=0.6V*(1+30.1K/20K)=1.503V

Security Classification	Compal Secret Data		
Issued Date	2015/08/10	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **PCH**

Size	Document Number	Rev
Custom	SKL_H 42	1.0

Date: Friday, August 14, 2015 | Sheet 59 of 62

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	41	Add DGPU_PWR_EN to EC pin71 Reserve LAN_WAKE# test point at EC pin66 Add R830 PU 10k to 3VALW for EC_LAN_WAKE#	04/07	SIV
2	HW design	9	add TC255~260 on UC1.B2, UC1.B38, UC1.BP1, UC1.BR2, UC1.C1, UC1.C38 TestPoint for SMT test	04/08	SIV
3	HW design	18	remove RH73, CH30 for DCPDSW_1P0 is output pin	04/08	SIV
4	HW design	36	add RC190 for CPU_XDP_TDO PULL high	04/08	SIV
5	HW design	17	RH105 stuff for KB_RST# is OD	04/08	SIV
6	HW design	42	JEDP1 conn. Pin define update	04/08	SIV
7	HW design	35	R228 stuff for novo_btn#	04/08	SIV
8	HW design	16	Change ch19, ch20 to 8.2p for meet X'tal spec	04/09	SIV
9	HW design	31	Change CL165, CL166 to 10p	04/09	SIV
10	HW design	42	C289,R334,C292,R335,C290,C291,U22 circuit change to R120,U5,C128,C1313	04/09	SIV
11	HW design	18	RH66,RH67,RH71,RH72,RH75,RH76,RH78 ,RH79,RH80,RH81,RH82,RH83,RH84 change to short pad	04/10	SIV
12	HW design	32	RC62 change to short pad	04/10	SIV
13	HW design	34	RA96,RA97,RA99,RA100 change to short pad	04/10	SIV
14	HW design	42	R336,R337,R333 change to short pad	04/10	SIV
15	HW design	8	RC83 change to short pad	04/10	SIV
16	HW design	11	RD3,RD5 change to short pad	04/10	SIV
17	HW design	38	R280 chagne to short pad	04/10	SIV
18	HW design	39	R281,R295 chagne to short pad	04/10	SIV
19	HW design	35	R230 change to short pad	04/10	SIV
20	HW design	33	R235~R242 change to short pad	04/10	SIV
21	HW design		RC43,RC49,RC54,RC57,RC81,RC83,RC189,RD4,RD8,RD12,RD22 ,RD26,RD28,RH36,RH51,R208,R323,R324,R314,R322,R331 ,RH40,RH42,RH43,RH46,R350,RA98 change to short pad	04/10	SIV
22	RF recommend	13	Add CH277,CH278 (@RF@)	04/16	SIV
23	HW design	40	RC142 change to 100kohm, add C1314(0.1u) for meet tCPU03	04/17	SIV
24	HW design	9	Delete TC257	04/20	SIV
25	HW design	10	Add TC263,TC264	04/20	SIV
26	RF recommend	11	Add CD271, CD272 for RF request	04/20	SIV
27	HW design	35	Update I/O board pindefine	04/21	SIV
28	EC recommend	15	Add RH108 reserve AC_PRESENT between EC and PCH	04/24	SIV
29	HW design	18	Add RH106(@),RH107	04/24	SIV

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
30	HW design	38	EC pin1 EC_LAN_WAKE# chagne to pin19, pin19 MPHY_EXT_PWR_GATE change to pin38 delete pin64 VCIN1_BATT_DROP, DCHG_I change from pin76 to 64pin	06/01	SIT
31	HW design	18	add RH118 between +3V_PCH and +3V_HDA for intel sighting 16 change RH80 from short pad to 0ohm and add CH279 for +1V_HDAPLL for intel sighting 16	06/01	SIT
32	HW design	32	R249 change to 4.99k, R263 change to non-stuff for HDMI EA R332,R244,R359,R250,R360,R361,R362,R363 change from 8.2ohm to 10ohm, R303,R304,R305,R306 change from 150ohm to 300ohm for HDMI EA	06/05 06/08	SIT SIT
33	EMI design	37	CA208, CA209, CA210, CA211 change to 680p and stuff for EMI request		SIT
34	RF design	40	add C1315 for RF request	06/09	SIT
35	RF design	45	Jadd C1316 for RF request	06/09	SIT
36	RF design	30	add CV525,CV527, for RF request	06/10	SIT
37	RF design	28	CV392 change to 22p for RF request	06/10	SIT
38	RF design	29	CV426 change to 22p for RF request	06/10	SIT
39	RF design	31	add CV526, CV528 for RF request	06/10	SIT
40	EMI design	37	RA5 change to 300ohm bead for EMI request	06/22	SIT
41	HW design	6	PEG change to Lanes 8:15 / DEVICE0 (544924_544924_Skylake_EDS_Vol_1_Rev_0.99)	06/22	SIT
42	ESD design	41	D3 change to SCA00001G00 for ESD request	06/22	SIT
43	ESD design	43	D21, D22 change to SCA00000U10 and stuff D16, D17 change to SC300002C00 and stuff	06/25	SIT
44	HW design	14	Cardreader change port from port17 to port11 Lan change port from port18 to port12	07/10	SIT2
45	RF design	40	add CLIP1~6 for RF request	07/14	SIT2
46	HW design	41	LED1 change to PULL HIGH to +3VLP	07/27	SIT2
47	EMI design	36	CL170, RL61, CL169, DL1 change to EMI@	08/11	SVT
48	EC design	38	add R832 for no KBL function	08/11	SVT
49	EC design	40	R201, Q2, R202, Q1, C214 change to KBL@	08/11	SVT

2015/02/06

Page 57

PU1601 change power sloution from SY8003D to SY198DQNC

Page 52

PR906 change from 45.3 +-1% 0402 to 100 +-1% 0402

Page 54

Add PC1337(S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9)

Page 56

PR1519,PR1532,PR1550 change from 1 +-1% 0402 to 1 +-1% 0201

PR1527 change from 100K +-5% 0402 to 100K +-5% 0201

PR1501,PR1502,PR1504,PR1508,PR1510,PR1516,PR1517,PR1518,PR1520,
PR1529,PR1530,PR1531,PR1548,PR1549,PR1552 change from 10K +-5% 0402
to 10K +-5% 0201

2015/02/06

Page 47

PR412 change from 10_0402_1% to 0_0402_5%

Page 46

PR319 change from 10K_0402_1% to 100K_0402_1%

PR323 change from 12K_0402_1% to 120K_0402_1%

PR322 change from 10K_0402_1% to 0_0402_5%

Page 48

PC502 change from 0.22U_0402_10V6K to 0.1U_0402_25V6

PR501 change from 2.2_0402_1% to 0_0402_5%

Page 56

PR1554 change from 887 +-1% 0402 to 1.05K +-1% 0402

2015/03/16

Follow Power module design.

Page 46

PR328 change to non-mount

PC316 change from 2.2U_0805_25V6K to 2.2U_0603_16V6K

Page 48

PR501 change from 0_0402_5% to 2.2_0603_5%

PC502 change from 0.1U_0402_25V6 to 0.1U_0603_25V7K

Add PR513(5.1_0603_5%)

PC514 & PC515 change from 1U_0603_10V6K to 1U_0402_10V6K

2015/04/10

Modify for ADP_ID circuit

Page 44

Add PR107(0_0402_5%)

PQ101 , PR103 & PR104 change to non-mount

Modify for ADP_I circuit

Page 45

PR206 & PR208 change to non-mount

Change to 0 ohm R-short for part count reduce

Page 46

PR322 change to 0 ohm-short pad

Page 47

PR412 change to 0 ohm R-short

Page 53

PR1005, PR1006, PR1012, PR1015, PR1021 & PR1022
change to 0 ohm R-short

Consider power budget, It can change CHOKE size to 2520.

Page 51

PL801 change to 1UH +-20% 2.3A 2.5X2X1.2
FERRITE(SH000011S00)

3 cell battery design can reduce 1pcs bead in VGA CORE

Page 56

Delete PL1502

2015/04/14

For CPU transient fine-tune

PC904 change from 0.039U_0603_25V7(SE00000A780)
to .01U 50V K X7R 0402(SE074103K80)

PR902 change from 1K_0402_1%(SD034100180)
to 12K_0402_1%(SD034120280)

PR913 change from 19.6K_0402_1%(SD000003580)
to 47.5K_0402_1%(SD034475280)

PR912 change from 8.45K_0402_1%(SD000000680)
to 19.1K_0402_1%(SD034191280)

PR920 change from 34.8K_0402_1%(SD034348280)
to 35.7K_0402_1%(SD000007D00)

PC901 change from 1000P_0402_50V7K(SE074102K80)
to 2200P_0402_50V7K(SE074222K80)

PR910 change from 1K_0402_1%(SD034100180)
to 2.32K_0402_1%(SD00000WS80)

PR933 change from 22.6K_0402_1%(SD034226280)
to 23.7K_0402_1%(SD034237280)

PR935 ,PR939 change from 1K_0402_1%(SD034100180)
to 590_0402_1%(SD00000CO80)

PR934 change from 3.3K_0402_1%(SD00000GW80)
to 4.7K_0402_1%(SD034470180)

PC918 ,PC922 change from 2200P_0402_50V7K(SE074222K80)
to 3300P_0402_50V7K(SE074332KL0)

PR966 change from 52.3K_0402_1%(SD034523280)
to 54.9K_0402_1%(SD00000H880)

PR964 change from 42.2K_0402_1%(SD034422280)
to 44.2K_0402_1%(SD034442280)

PR940 change from 3.3K_0402_1%(SD00000GW80)
to 4.12K_0402_1%(SD034412180)

For sourcer request,modify P/N

PC1001,PC1006,PC1013,PC1017,PC1029,PC1030 change
from SE000005ZL0(0.22U 25V K X7R 0603)
to SE000005Z80(0.22U 25V K X7R 0603)

PC602 ,PC802 change
from SE000008L80(22U 6.3V M X6S 0805 H1.25)
to SE00000M000(22U 6.3V M X5R 0603)

PC203,PC204,PC312,PC402 change
from SE075103K80(.01U 25V K X7R 0402)
to SE074103K80(.01U 50V K X7R 0402)

PC505 ,PC506 change
from SE093106K80(10U 6.3V K X5R 0805 H1.25)
to SE000005T80(10U 6.3V M X5R 0603 H0.8)

PC1007,PC1008,PC1018,PC1020,PC1031,PC1032 change
from SE107225KL0(2.2U 6.3V K X5R 0603)
to SE000008880(2.2U 6.3V M X5R 0402)

To avoid leakage current at +1V_VCCST.

PR932 change to non-mount

Base on test result,reduce CPU output cap.

PC927 change to non-mount

PC1103 ,PC1105 ,PC1106 change to non-mount

PC1117 ,PC1113 ,PC1116 ,PC1109 change to non-mount

PC1146,PC1147,PC1148,PC1149 change to mount

For HW request,modify power sequence.

PC517 change from SE102104K00(0.1U_0402_10V7K)
to SE074102K80(1000P_0402_50V7K)

PC1401 change from SE076104K80(0.1U_0402_16V7K)
to SE074102K80(1000P_0402_50V7K)

VGA CORE component over heat issue,change to
AON6970 to reduce power loss.

PQ1501 ,PQ1502 ,PQ1503 change from SB00000XJ10(AON6932A 2N DFN5X6-8)
to SB000010K00(AON6970 2N DFN5X6D)

2015/04/30

Force VGA core work in 3-phase CCM mode.

Add PR1524 (10K +-1% 0201)

Add snubber and 6.8pF cap for EMI and RF request

Add PR405 & PR411 (4.7_1206_5%)

Add PC412 & PC428 (680P_0603_50V7K)

Add PR1007.PR1008.PR1016.PR1014.PR1023.
PR1024 (4.7_1206_5%)
Add PC1009.PC1010.PC1021.PC1019.PC1033.
PC1034(680P_0603_50V7K)

Add PC704(6.8P_0402_50V8C)

Add VGA VR_TT# protection circuit
to VGA AC_batt (GPIO 5)

Add PR1610(100K_0201_5%)

Add PQ1504(DMN65D8LDW-7_SOT363-6)

Modify for ADP_ID circuit

Delete PR107(0_0402_5%)

2015/06/01

Follow Power module design.

PR309 & PR310 change from 10 ohm to R-short

Reduce part count for 3S battery design

Delete PR221 and PR225

Reduce part count

PR904,PR909,PR916,PR921,PR923,PR924,PR925,PR929
,PR976,PR977,PR978 change to 0-ohm R-short

PR1514,PR1511 change to 0-ohm R-short

Base on power budget ,modify solution

PU1401 change to SYX196DQNC

2015/06/05

Reduce part count

PR313,PR317,PR320,PR511,PR1409,PR1605 change to 0-ohm R-short

Skylake RTC circuit modify

Add PR107(45.3K_0603_1%)

Add PR105 change from 1K_0603_5% to 1.5K_0603_5%

2015/06/08

Reduce part count

PR1003,PR1013,PR1020,PR1004,PR1011,PR1019 change to
0805 0-ohm R-short

PR314,PR404,PR410,PR704,PR1404, PR1522,PR1542
PR1604 change 0603 0-ohm R-short

EMI & RF request

Add PR325(4.7_1206_5%) and PC320(680P_0603_50V7K)

PR316 change from 0_0603_5% to 2.2_0603_5%

Reserve PC1615(6.8P_0402_50V8C)

2015/06/22

For RF noise issue

Change CPU cap location from PC1101 & PC1102 to
PC1103 & PC1105

Delete PC1101 & PC1102

For CPU transient fine-tune

PR913 change from 47.5K_0402_1% to 48.7K_0402_1%

PR933 change from 23.7K_0402_1% to 23.2K_0402_1%

PC928 change from 1000P_0402_50V7K to 1200P_0402_50V7K

2015/06/22

For PU1601 OTP issue

Change PL1602 to 0.8UH_MND-05BZIR80M-
XBL_12A_20%(SH00001BV00)

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